Monday to Thursday

- Completion of the thesis
- Finalization of the written report.

Friday

- Report hand in
Monday

- Function to generate random masks for correlations
- Test random mask generator: baseline observable, but much smaller compared to test beam data

Tuesday

- Repetition of 3ptGain test without and with trim
- Thesis: documentation of telescope-Correlator match, improvements of correlator, first characterizations
- Thesis: revise chapter 2 & 3

Wednesday

- Documentation of 3 Pt gain and trimming.

Thursday

- More test with random correlation generator
- Documentation of random generated correlations

Friday

- Further analysis of random correlation generator
- Presentation at student meeting about test results

→ Tasks for the next week

- Finalize thesis
Monday

- Data analysis and comparison with simulations
- Noise run: measurement of noise/random generated correlations.

Tuesday

- Response curve measurement started
- Thesis: discussion of simulated address distribution

Wednesday

- FPGA design version with 40MHz BC and 320MHz FCLK. For single chip test by Jonas Stalder.
- Response curve measurement finished for one side.

Thursday

- Thesis: documentation of doublet construction
- Thesis review and corrections

Friday

- Threshold scan analysis and documentation
- Thesis: review and corrections

→ Tasks for the next week

- Random correlation generator
- Thesis completion
Self-seeded Trigger

Tracking with self-seeded Trigger for High Luminosity LHC

Weekly work report

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Monday

• Todo list for different analysis and other task created
• Plots for \( \mu \)m-pos scan
• Thesis: description of test beam setup

Tuesday

• Plots for \( \mu \)m-pos and threshold scan
• Thesis: test beam measurement descriptions

Wednesday

• Plots for threshold scan and address distribution
• Small presentation with results so far
• Thesis: result and analysis of \( \mu \)m-pos

Thursday

• Test beam meeting, where I presented some results
• Plots for address distribution and derivative of threshold scan
• Thesis: results and analysis of beam spot and address distribution
• Started 3pt gain with trimmed doublet

Friday

• Beam profile and address distribution analysis and documentation
• Repetition of 3pt gain with andouguh trim. One side failed and the measurement has to be repeated

→ Tasks for the next week

• Data analysis and simulations
• Thesis writing
Monday

- Haichen Wang analyzed the data from the correlation and found a peak in the distance distribution.
- The flat distance distribution previously observed comes from false correlations (tracks of two particles resulting in a correlation).
- Night session to scan over micrometer position. Observed movement of distance in the correlations

Tuesday

- Conclusion of test beam measurements.
- Remove setup from end station A.

Wednesday

- Thesis: Description of correlator test system

Thursday

- Thesis: Description of correlator test system
- Simulation of random correlations

Friday

- Data analysis

→ Tasks for the next week

- Data analysis
  - Schedule and plans for conclusion of the work
Monday

- Correlation measurements
- Improvements in the test system

Tuesday

- Threshold scan measurement

Wednesday

- Beam was off during the day
- Simulation of hit pattern generated by the FCF, if multiple hits on one chip. The patterns observed could be reproduced.

Thursday

- Event based readout. MB collects correlations and sends them together with the trigger back to LabVIEW
- Threshold scan measurements with beam
- Started to scan over micrometer position. No shift in distance could be observed after moving by 150 μm so far
- Thesis: description of doublet frame

Friday

- Micrometer scan was continued by Jonas Stalder, John Keller and Jacob Pasner
- Because no change in the correlation, frame was opened and it was observed, that the micrometer did not move the mobile part
- Started simulation for correlation distance

Sunday

- Control and adjustments to the movement control of the doublet
- Measurements with moving mobile part of doublet, no change in distance found
- Check of code and search for logic error to explain why flat distance profile
→ Tasks for the next week

- Conclusion test beam
- Analysis
Monday

• Correlation measurements
• Improvements in the test system

Tuesday

• Threshold scan measurement

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• Check of code and search for logic error to explain why flat distance profile
Tasks for the next week

- Conclusion test beam
- Analysis
Monday

- Meeting regarding SLAC test beam and planning of doublet construction
- TLU: further tests and logic modifications to prevent the busy signal to hold
- Hybrid # 3 bond corrected and successfully tested
- Glued hybrids on sensors

Tuesday

- TLU communication successfully tested. Can now receive the trigger ID.
- First hybrid was bonded to sensor. One row has too long bonds and many of them had to be removed or are touching together.
- First sensor glued to frame.

Wednesday

- Mobile side of doublet completely bonded.
- Measured IV curve of sensor
- Could successfully access the ABC130 chips on the first hybrid
- Glued static side sensor

Thursday

- Finished bonding of doublet
- Test of the complete doublet. Possible to read all chips

Friday

- Test and analysis of doublet
- Final preparations for SLAC test beam.
- Decided to go on Saturday

Saturday

- Installation of the setup in ESA at SLAC
- Test of the readout system, all chips can be read back
Sunday

- Improvements of the readout system
- First correlations observed

\(\rightarrow\) **Tasks for the next week**

- Measurements at SLAC
Monday

- LabVIEW program improvements
  - timestamps when reading data from serial port
  - save, read and auto plot of correlation, trigger and FCF data
  - interface for data file creation

Tuesday

- Meeting for the SLAC test beam organization
- verification of LabVIEW arrival timestamps, are working well. Not very precise measurement of arrival time, but tags sent together should be within a couple of milliseconds.
- Correlator output logic modified to insert delay before adding trigger ID.

Wednesday

- FCF auto readout implemented. Whenever some FCF data are received (not 0xFFFFFFFF) it is stored in the FCF output FIFO and the MB sends it to the computer.
- Hybrid boards will be mounted on doublet frame for testing.
- TLU arrived and started to install software.

Thursday

- Assembled ABC130 chips on 3rd hybrid, because the first can’t be used for bonding anymore.
- Test of TLU: problems installing the software to control the TLU
- Planning for hybrid to sensor glueing

Friday

- Interface board HW modification to have TLU connector
- Test of TLU: receive trigger signals, but read Trigger ID’s don’t look correct yet.
- Hybrid # 3 was bonded and tested. Chip 7 has one broken bond on the FCLK and therefore can’t be read out correctly.
- Test hybrid glued onto mechanical sensor for bonding tests.
Tasks for the next week

- Glue hybrids onto sensor
- TLU trigger input test
- Test beam preparations and start
Monday

- LabVIEW interface improved (configuration settings, initialization function etc)

Tuesday

- Thesis: description of correlator design

Wednesday

- Thesis: description of correlator design
- Online training for SLAC
- Discussion about test beam organization

Thursday

- Design and implementation of TDC to measure arrival time of the trigger input
- First stage of TDC with counter realized

Friday

- Implementation of second stage TDC with delay elements, based on a design by Martin Kocian.
- Tests of TDC: 1st stage works, 2nd stage is not yet giving the output as expected.

→ **Tasks for the next week**

- Preparations for test beam
- LabVIEW program updates and functionality improvements
- Test of TLU and trigger arrival
Monday

- Added ODELAY element to FCLK outputs.
- Now the phase shift for the 20MHz setup is also correct and the delay issue is not present.
- Started to scan ODELAY values to confirm FCF logic dependency on phase between FCLK and BC.

Tuesday

- Verified dependency of FCF to FCLK and BC. Two stable ranges of the phase.
- Started design for trigger input from TLU for test beam

Wednesday

- Implementation of interface to EUDET TLU
- Tested on HW with push button as trigger input signal and output signal confirmed on scope.
- Prepared presentation for Friday student meeting.

Thursday

- LabVIEW application created to read data output from correlator.

Friday

- Analysis of data in LabVIEW application added.
- Plotting stubs on XY graph for control, possible to save information for post-analysis.
- Progress presentation at the students meeting

→ Tasks for the next week

- Test communication with TLU
- complete association of trigger ID with correlator tags
Monday

- Update of correlation output logic, so that no trigger signal is needed to generate data.
- Input delay on FCF lines to delay each line by one BC period.
- Each input IDELAY configurable individually.
- RTL schematic update and general code revision.

Tuesday

- Simulation of revised code and correction of minor errors
- Could successfully test correlation with calibration pulse input. But only on reduced set of ABC130s, due to delay problems.

Wednesday

- Test of design with 10MHz BC clock. Problems with FCF readout, but no delay. When switching back to the 20MHz design, also no delay present.
- Could successfully configure and read all 20 chips in parallel.
- Successful test of the correlation logic on the complete doublet.
- Still delay problem, when loading directly the 20MHz design.

Thursday

- Found reproducible instructions to get running setup as well as delayed setup.
- 1.) Power on system 2.) Program FPGA with 10MHz design 3.) Send FCF reset 4.) Program FPGA with 20MHz design 5.) Functional FCF readout with no delays 6.) Send FCF reset 7.) Non-functional FCF readout with delay issue 8.) Repeat steps 2 to 7
- The phase between the FCclk and BC is different for the 10MHz and 20MHz design.

Friday

- Out of office - visit of UC Irvine
→ **Tasks for the next week**

- Analyse effect of phase between FClk and BC to have a functional 20MHz design
- Trigger integration for test beam according to [1]
Monday

- Memorial Day

Tuesday

- Reasearch on offset problem: Known as “baseband wander”, which is caused by an non-DC balanced signal. This is here the case because the FCF line is always at ’1’, if no data arriving. AC coupling is therefor not recomended [2, p.2]
- Removed capacitor from AC coupling from the SLVDS to LVDS conversion. → offset disappeared.

Wednesday

- Function to automatically set phase shift and IDELAY values written and tested.
- It’s possible to adjust correctly the first build hybrid, so that all lines can be read at the same time.
- Hybrid #2 not yet possible to set the delays. Still the same problem on the first three chips.
- Correlation test with input, where chips with delay issues are not used. No output so far from the correlator.
- Timing adjustment on hybrid #2 not possible with long cable

Thursday

- Some unsuccessful tests with the ground configuration
- Improvement of auto-phase shift set function.
- Thesis: section about modifications and problems encountered on the FCF test system

Friday

- Mitch Newcomer, developer of the FCF cluster finder, was in Berkeley and helped to analyze the delay problem.
- The reason behind the problem is not yet solved, but we go a better understanding of the system.
- Other test that can be performed are:
Self-seeded Trigger

- Measure the effect of the supply voltage
- Scan the FCF driver current
- Stability test of the readout over a longer time

- The delay should be adjustable individually for each FCF line and not only for each chip.

→ **Tasks for the next week**

- Test of correlation with reduced set (ignore chips which can’t be matched)
- IDELAY configurable for each line
Monday

- Implemented IDELAY on FCF input lines. Possible to adjust the delay on each channel by $\sim 2.5$ ns.
- Problem on FCF lines, because large delay between the chips

Tuesday

- Having still problems reading the FCF lines. Observe strange behaviour, like delay between FCF lines from the same chip.

Wednesday

- Still observing delays between the FCF lines.
- Tried with old FPGA bitstream, but problem occurs also there.

Thursday

- Worked on delay issue on FCF lines
- Tried to find steps to reproduce certain delays, but they seem to appear randomly after probing for signals.
- Carl supposes an issue with the differential lines

Friday

- Probed differential lines and found another issue: At the input of the SLVDS to LVDS is an offset on the differential signal.
- The offset is only present when the ABCs are in operational FCF mode. In framing mode the signal arrives correct. I suppose an issue with the AC coupling, which is not necessary according to the datasheet of the LVDS driver.

→ Tasks for the next week

- Fix offset and delay problem
- Automatic setup of phase shift and IDELAY
- Correlator test
Monday

- Worked on correlator control program for MB.
- Prepared power cable for bottom hybrid.

Tuesday

- Communication possible with both hybrids at the same time.
- FCF readout working and some responses from correlation logic. When the FCF output is off, the FCF lines are kept at '0' which is a valid hit information. The correlator output is not correct to this though.
- Bottom FCF lines have improper signal because the bottom FCLK output signal from the FPGA has a low amplitude and is not propagated correctly.
- Input pins from chip 6 FCF line 1 were wrong

Wednesday

- Worked on the MB program
- Chip 6 FCF line 1 working now
- Still problem with bottom FCLK. Try to use different output (for FCF emulation)
- RTL schematics updated

Thursday

- Found alternative line for bottom FCLK and made cable for the fix.
- Bottom signals look now correct (framing and mask mode).

Friday

- Correlation logic successfully tested with ABCs in masked mode. (only partial input used).
- FCF input lines need IDELAY block to read correctly all lines at the same time
- ABC9 on new hybrid exchanged and now working.
- Problems with FCF readout in with calibration pulse
Tasks for the next week

- Add IDELAY on FCF input lines
- Fix problem with FCF readout on calibration pulse
Self-seeded Trigger

Tracking with self-seeded Trigger for High Luminosity LHC

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<td>Niklaus Lehmann</td>
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<td>05.05. - 09.05.2014</td>
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Monday
- Concept and documentation for correlator readout (RTL schematics)
- Discussions for doublet production

Tuesday
- Implementation of correlator readout and simulation

Wednesday
- Successful simulation of complete correlator system (except MB)
- Synthesis possible, but high data path delay on "find_first_valid" logic, which is used to select the valid tags and stores them in the correlator output FIFO. Reduced frequency for tag store to match path delay.
- First concept for new MB code

Thursday
- Correlator system loaded into FPGA
- Started to write MB program to read values from the correlator logic
- 2nd Hybrid on support board mounted

Friday
- Test of 2nd Hybrid. All but chip 9 are responding (might be a defective chip).
- MB correlator control program continued. Possible to communicate with ABC130s with correlator system.

→ Tasks for the next week
- Complete correlator control program
- Test of bottom hybrid readout
- Test of correlator logic
Monday

- Finalized simulation of full hybrid correlator logic.
- Started with filter and serializer block to select only the valid tags as output from correlator.

Tuesday

- Work on correlator output logic.
- Analysis of output data to be stored.

Wednesday

- Work on data filter and correlator output logic
- Visit of SLAC test beam

Thursday

- Work on correlator output and communication with PC
- Correlator logic and storage in FIFO functional and tested with simulation.

Friday

- Nygren Symposium

→ **Tasks for the next week**

- Correlator on FPGA: data readout with PC
- Preparations for test beam
Monday
- Recreated system with only 320MHz output
- Integration of correlator
- Report: description of correlator

Tuesday
- Simulation of simple correlator bloc to reproduce L. Pirramis results
- Still struggling with timing optimization

Wednesday
- Working system at with 320MHz max FCLK. Needs more testing to see if always working. In the timing optimisation process, a software reset of the counter for the cmd for the output data was forgotten. Which resulted in a to far delayed last_bit signal.
- Infrared images of hybrid board, to check if cooling will be necessary. → chips have max. 40°C and no cooling necessary
- Report: correlator description

Thursday
- Redesigned top level to have one single MMCM for the clock generation and to separate the MicroBlaze from the rest. Allows a simpler simulation of the complete logic.
- Test bench for total interface created
- Have now a system that works stable (so far).

Friday
- Correlator interface written
- Modification in connecting the input values, considering the flipped bottom module. Chip and strip address order is inverted.
- Simulation of whole correlator
Tasks for the next week

- Correlator on FPGA
- SLAC test beam introduction
Monday

- Response curve for ABC1. Similar as ABC0 slightly more noise
- Timing analysis of FPGA design. Timing diagram for new FCF deserializer bloc created.
- Microblaze frequency: timing constraints better matched with 80MHz, but serial port not working due to incorrect output frequency. Decided to go with 160MHz, where the serial port works.

Tuesday

- New FCF deserializer bloc implemented in VHDL and tested with Modelsim

Wednesday

- FPGA timing optimization
- study of correlator logic and functionality

Thursday

- FPGA timing optimization
- started specification for higher level track correlator
- started implementation of correlator logic into FCF test system

Friday

- FPGA timing optimization
- Integration of correlator logic into system

→ Tasks for the next week

- Correlator on FPGA
- terminate timing optimizations, probably reduce max speed to 320MHz
Monday

- FPGA timing analysis
- Optimization of FCF deserializer bloc

Tuesday

- Timing optimization on FCF deserializer bloc
- Timing analysis on LabVIEW interface. Found that the VISA clear uses most of the time. This VISA is essential for a correct communication and can’t be removed directly.

Wednesday

- Timing analysis of FPGA project
- Study of correlator functionality

Thursday

- Timing analysis of FPGA project
- Ideas for higher level correlator
- Report: ABC130 commands and trigger

Friday

- Timing analysis and optimization of FPGA project
- Clock tree analysis and optimization

→ Tasks for the next week

- Clock tree optimization and constraints settings
- Correlator on FPGA
- Characterization of further ABC chips
Monday

- Analysis of FPGA timing and other suggestions from Réne Beuchat

Tuesday

- Threshold scan measurements and analysis
  - Gain found 28 mV/fC @ 1fC ← too low, should be 60-70 mV/fC
  - Noise found 1200 e ← too high, should be around 400 e

Wednesday

- Created function to scan Strobe Delay. According to input from Bruce, this could help to improve the measurement.
- Repeated threshold scan measurements
  - Gain found of 65 mV/fC @ 1fC ← looks ok
  - Noise found 600 e ← still to high, but looks better

Thursday

- Created function for response curve measurement
- Measurement of full 10 point gain overnight.
- Report: chapter for ABC130 test system started, description of calibration tests.

Friday

- Analysis of 10 point gain measurement → promising results, gain too low and noise a little too high. Most importantly test takes too long
- Summarizing possible solutions to speed up measurements
  - Integrate averaging function in MicroBlaze instead of LabVIEW
  - reduce amount of measured threshold values and fit measured points to known function
- Analysis of the FPGA clock signals.
- Report: continued chapter on ABC130 test system.
Tasks for the next week

- Complete timing constraints for FPGA system
- Correlator on FPGA
- Characterization of further ABC chips
Monday

- Tried to implement strobe delay test with LabVIEW
- Studied ABC130 spec to define registers to be set
- Problem with synchronizing pulse to inject test charges

Tuesday

- Could trigger charge injection and synchronized FCF readout to get the results. Thanks to Bruce Gallop for input.
- Modification of the programmable delay block in the ABC130 Tester. Needs a longer delay than currently available.

Wednesday

- Development of threshold scan function.

Thursday

- First threshold scans performed on four pairs of channels. Readout of one FCF value takes about one third of a second. → might be interesting to implement a readout function in the MicroBlaze.
- There is still quite a problem with the alignment of the input data. It works but in a large set there are several that fail to be read correctly.

Friday

- Automatic delay scan to find working phase shift value for FCF readout
- Performed further threshold scans and some first calculations about noise level.
- Writing ABC130 chapter for report

→ Tasks for the next week

- Further Threshold scans.
- Threshold scan on MicroBlaze. Compare work with gain for decision.
- Perform readout of complete chip
- Study of correlator logic and start test
Self-seeded Trigger

Tracking with self-seeded Trigger for High Luminosity LHC

Weekly work report

| Niklaus Lehmann | Date       | 17.03. - 21.03.2014 |

Monday

- Received fix for phase shift bloc from Lorenzo. Now the delay for the FCF readout is working.
- Collecting references about trigger system, [3]

Tuesday

- Work on FCF readout with LabVIEW.
- Found that the FCF lines are inverted on the connection from the support board to the IB.
- With the correct phase shift it is possible to read the values correctly.
- The phase shift for the FCF readout has to be done for each chip.

Wednesday

- I inverted the signal on the FPGA and now I see the correct values in LabVIEW.
- Added two more ABC130 chips and could successfully test both.

Thursday

- Worked on updated LabVIEW interface for automatic FCF readout and test
- Glued last five ABC130 chips on hybrid and Rhonda will do the wirebonds.

Friday

- Tested last five ABC130. Chip 6, 7, 8 & 9 are responding correctly. Chip 5 changes voltage when setting LDOD, but no output on FCF lines. On Chip 6 FCF1 it looks like the termination resistance is not working correctly.
- Continued work on LabVIEW interface for automatic FCF readout. Tested successfully a readout of all FCF lines with constant delay (using Mask register as input).
- Finished introduction chapter of report.
→ **Tasks for the next week**

- Define setup to perform test charge injection and readout of the channels.
- Study resources and start thinking about concept for high level correlator
- Report: Description of ABC130 chip
Monday

- ABC130 chips respond and measured all voltages on AMUX and regulated supply voltages.
- ABC130 Tester modification to set ABC address in LabVIEW interface.
- Tested access of FCF readout interface. Got some data back, but have to check if its correct.

Tuesday

- Could successfully verify data received through the FCF lines.
- Measured with 18ns a higher delay in the framing mode than expected.
- Comparison of voltage levels to single chip setup and found similar values.
- Prepared presentation for student meeting on Friday.

Wednesday

- Tried readout of FCF data with LabVIEW, but unable to capture the correct data.
- Problems with phase shift block to align BC clock with received data. Not possible to modify phase shift.
- Deformed signal after LVDS driver on IB because internal termination resistances on FPGA were not activated → corrected.

Thursday

- Visit to Santa Cruz

Friday

- Student presentation about the goals
- Skype with Lorenzo, he tries to simulate phase shift for FCF readout.
- Looking into synthesis reports and compilation warnings to understand better what the configuration needs to be for a correct functioning system.
- Discussions about mechanical setup for doublet.
Tasks for the next week

- Collect references for higher level correlator and start to study them.
- Set constraints to have a working ABC130 test system.
- FCF readout with LabVIEW.
## Tracking with self-seeded Trigger for High Luminosity LHC

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### Monday

- Connected power for ABC130 on single chip board.
- Could write the register and observe a change on the AMUX output pin and also for the LDOD and LDOA
- Found that the reference voltage is not correct on driver board → needs change of R26/R27
- ADC lines to measure LDOA and LDOD appear to be inverted

### Tuesday

- ADC lines ok, looked at an old schematic. VREF also correct at 2.449V.
- Successful readout of both ABC130 single chip boards. Error was old firmware on driver board and incorrect configuration files for SCTDAQ

### Wednesday

- Probed signals and commands sent to ABC130 on single chip board to have a known good sample. Saw that the voltage levels appear to be LVDS at the input of the ABC130 instead of expected SLVDS levels.
- Started to probe signals on ABC130 test system (interface board and hybrid). Problems because unstable signals on SLVDS. Need to use differential probes.

### Thursday

- Continued probing on ABC130 test system. BC clock, RCLK and L1R3 signal present and with correct LVDS levels.
- Wasn’t able to capture reset or long command signals on the COML0 line.
- LO is present and small error with ACK signal to LabVIEW interface corrected.

### Friday

- Skype with Lorenzo but couldn’t find problem why COM signal can’t be captured.
- As suggested by Lorenzo, I modified FPGA project to have internal signals from the COM generation bloc on test outputs, after that I managed to probe all signals and verified them successfully with the signals from the single chip board.
- Now also the change of the regulated voltage output, as well as the AMUX was possible.
Self-seeded Trigger

- Has to be confirmed on Monday
- Thesis report, general layout update and introduction about LHC and ATLAS.

→ **Tasks for the next week**

- Confirm correct function of sending commands to the ABC130 chips on hybrid
- Access independently the chips
- Start with FCF test
### Weekly work report

**Week 1**

**Niklaus Lehmann**

**Date** 24.02. - 28.02.2014

**Monday**

- Introduction to the lab and visit of the working place.
- Carl had a talk in the afternoon, so the detailed introduction was postponed.
- Read the report of Lorenzo Pirrami [5], the preceding master thesis.

**Tuesday**

- Finished reading report [5]
- Getting used to the ABC130 Test System from Lorenzo. After a first successful run, there were problems in the communication between LabVIEW and the FPGA (MicroBlaze).
- Brief discussion about the next steps at lunch with Carl and Sergio:
  - get familiar with Lorenzos work
  - make ABC130 chips, mounted on single test print work

**Wednesday**

- Study of ABC130 specifications [6]
- Working with ABC130 Test System, communication problems solved. Was because of unproper shutdown of Test Environment. Make sure to stop LabVIEW program before switching off FPGA. In case of problems, close LabVIEW completely to free serial port.

**Thursday**

- Test with ABC130 tester. Could prob different signals (BC, FastCLK, L1R3 trigger) with scope, but no signals on L0_COM.
- No ACK when L0 trigger is sent to LabVIEW
- Instructions received regarding installation for ABC130 test on HSIO

**Friday**

- Setup for the ABC130 single chip board.
- Possible to configure the HSIO and the driver board, but no access to the ABC130 yet. Probably lacking power sources.
- Discussion with Carl about the project goals → see first draft of thesis report
**Glossary**

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<tr>
<td>μm-pos</td>
<td>Micrometer position for test beam.</td>
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<tr>
<td>ABC130</td>
<td>new ATLAS Binary Chip in 130nm technology.</td>
</tr>
<tr>
<td>AMUX</td>
<td>Analog Multiplexer Output on ABC130.</td>
</tr>
<tr>
<td>BC</td>
<td>Beam Crossing clock.</td>
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<tr>
<td>ESA</td>
<td>End Station A, arrival hall of test beam at SLAC.</td>
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<tr>
<td>EUDET</td>
<td>European Detectors, European program for detector research and development.</td>
</tr>
<tr>
<td>FCF</td>
<td>Fast Cluster Finder.</td>
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<tr>
<td>FCLK</td>
<td>FCF clock signal.</td>
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<tr>
<td>HL-LHC</td>
<td>High Luminosity Large Hadron Collider.</td>
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<tr>
<td>HSIO</td>
<td>High Speed Input/Output board.</td>
</tr>
<tr>
<td>IB</td>
<td>Interface Board, LVDS driver board between FPGA and support board.</td>
</tr>
<tr>
<td>IDELAY</td>
<td>Input delay bloc for FPGA input pins.</td>
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<tr>
<td>LDOA</td>
<td>ABC130 Analog Low DropOut Voltage regulator.</td>
</tr>
<tr>
<td>LDOD</td>
<td>ABC130 Digital Low DropOut Voltage regulator.</td>
</tr>
<tr>
<td>LVDS</td>
<td>Low Voltage Differential Signaling.</td>
</tr>
<tr>
<td>MB</td>
<td>MicroBlaze, softcore processor on Virtex 6.</td>
</tr>
<tr>
<td>MMCM</td>
<td>Mixe-Mode Clock Manager, FPGA element to create clock signals.</td>
</tr>
<tr>
<td>ODELAY</td>
<td>Output delay bloc for FPGA output pins.</td>
</tr>
<tr>
<td>SCTDAQ</td>
<td>Silicon Tracker Data Acquisition software.</td>
</tr>
<tr>
<td>SLAC</td>
<td>Stanfort Linear Accelerator Center.</td>
</tr>
<tr>
<td>SLVDS</td>
<td>Sub-LVDS, same as LVDS but with lower voltage levels.</td>
</tr>
<tr>
<td>TDC</td>
<td>Time to Digital Converter.</td>
</tr>
<tr>
<td>TLU</td>
<td>Trigger Logic Unit, from the EUDET telescope.</td>
</tr>
</tbody>
</table>
References


