Project Specification v4.6
Project Name: ABC130 ASIC

Date	Change	Author
April/03/11	DRAFT Document Begin	F.M.N.
	Much of the ABC information has been left in and **shaded** to preserve the Useful text in the document. Remaining text should be eliminated when this document goes from DRAFT to a Versioned ABC130 Specification Document.	
02/03/12	Major update including functional changes	F.A.
29/09/12	Major update with registers definition and Fast Cluster Finder description	F.A.
31/01/13	Updated Register Definition IO pads and other functional changes	F.A.
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18/02/13	EventBuffer Reset	F.A.
30/04/13	Updated registers description and pads definitions	F.A.
05/07/13	Added ABC130 pads geometry, various updates	F.A.

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PRELIMINARY STATEMENTS ABOUT THE DOCUMENT

The ABC130 specification is created from its predecessor the ABCn ASIC, it will be the third generation of the ATLAS Semiconductor Tracker (SCT) Readout:

ABCn ASIC Requirements and Specifications

ABCD3TA ASIC Requirements and Specification

ATL-IS-ES-0039

EDMS Id: **317413**

https://edms.cern.ch/cedar/plsql/doc.info?cookie=7245285&document_id=317413&version=1

http://scipp.ucsc.edu/groups/atlas/elect-doc/abcd3t_spec.pdf

The ABC130 significantly differs from the ABCn and predecessors. The main changes are listed below:

- 130nm CMOS technology
- 1.3V external power supply
- Three Trigger types, L0, R3 and L1 control the data flow.
- Fixed Length data structure with multiple data types.
- Xon / Xoff flow control between chips.
- Readout clock up to 160Mbits/sec.
- Readout mode compatible with an external Hybrid Controller Chip, HCC
- Bonding pads arrangement, chip size fitting to the hybrid prototype
- SEU errors handling
- I/O and register scan through JTAG
- Fast cluster finder logic

Comments, open issues, preliminary parameters or descriptions are printed in grey in this document.

1 SCOPE

This document describes the requirements and target design specifications for the front-end ASIC to be used in the binary readout architecture of silicon strip detectors in the ATLAS Semiconductor Tracker Upgrade. The ABC-130 chip is designed in the IBM CMOS8RF 130nm technology. The ABC-N design is based upon the ABCD3T-A chip used in the ATLAS SCT Tracker.

2 REFERENCE DOCUMENTS

1. Atlas Binary Chip (ABC), Project Specification, Version V4.03.
2. ABCD3TA ASIC Requirements and Specification, ATL-IS-ES-0039, EDMS Id: 317413
3. RAL 214 /DORIC3 Project Specification, V1.01.
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5. F. Campabadal, et al., “Design and performance of the ABCD3TA ASIC for readout of silicon strip detectors in the ATLAS semiconductor tracker”, Nucl. Instr. and Meth. A 552 (2005), 292-328.
6. J. Kaplon and W. Dabrowski, “Fast CMOS Binary Front End for Silicon Strip Detectors at LHC Experiments”, IEEE Trans. Nucl. Sci. TNS 52, No. 6 (2005), 2713-2720.
7. F. Anghinolfi, W. Dabrowski, Proposal to develop ABC-Next, a readout ASIC for S-ATLAS Silicon Tracker Module Design,
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9. Technical Specification: Supply of SiliconMicrostrip Sensors of ATLAS07 specification. July 2007.
10. Kaplon, J.; Noy, M.; , "Front end Electronics for SLHC Semiconductor Trackers in CMOS 90 nm and 130 nm Processes," Nuclear Science, IEEE Transactions on , vol.59, no.4, pp.1611-1620, Aug. 2012

3 TECHNICAL ASPECTS

3.1 Requirements

3.1.1 General

The chip must provide all functions required for processing of signal from 256 strips of a silicon strip detector in the ATLAS experiment employing the binary readout architecture. The simplified block diagram of the chip is shown in figure 3.1. The main functional blocks are: front-end, command decoder, input register, pipeline, event buffer, readout logic, threshold&calibration control, power regulation.

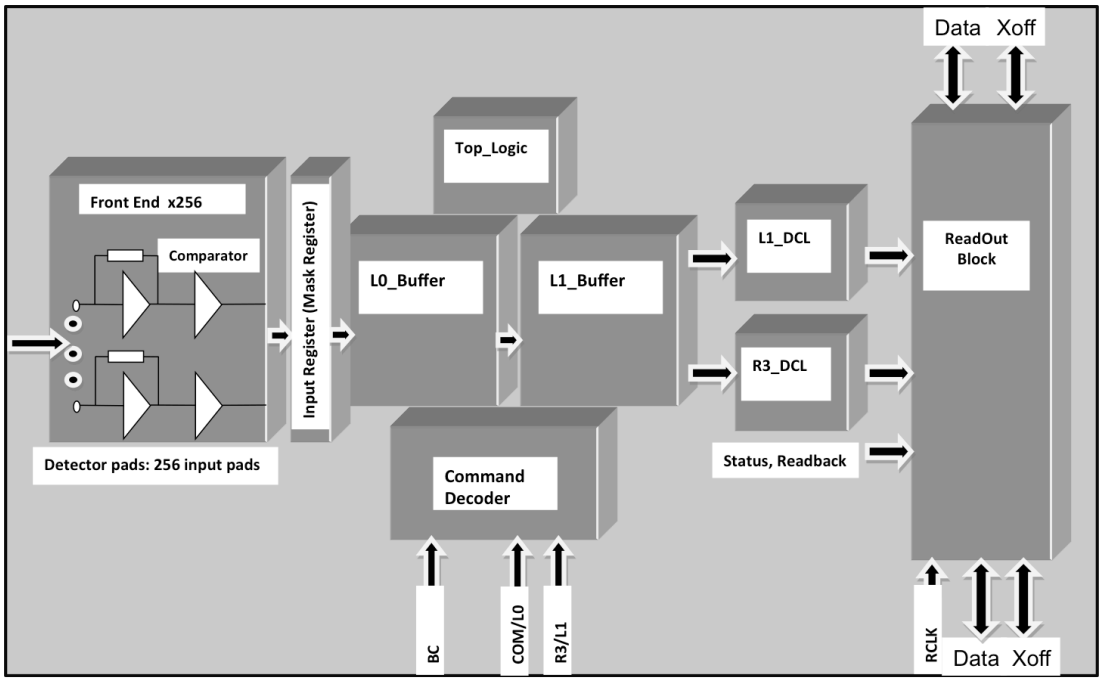


Figure 3-1 Block diagram of the ABC130 chip.

3.1.2 ABC130 Architecture

The new architecture chosen for the ABC130 allows a multi-trigger data flow control retaining the Beam Crossing synchronous pipeline transfer signal (L0 here) from previous versions and a new asynchronous Regional Readout Request (R3 here) and a second level asynchronous data readout intended for a global readout (L1 here).

3.1.2.1 Control Signals

The table below defines the ABC130 control signals.

Table 3-1 Control Signals

Name	Type	Description
In1- In256	Analog	Preamplifier Inputs from silicon strip sensors
FastCLK	SLVS	(320 or) 640MHz Clock input primarily intended Fast Cluster Finder
RCLK	SLVS	(80 or) 160MHz Clock input primarily intended for Data Readout
BC	SLVS	Beam Crossing Clock at 40MHz

L0_COM	SLVS	L0 Synchronous Trigger with BC falling edge, COM with BC rising edge
R3_L1	SLVS	R3L0ID with BC falling edge, L1L0ID with BC rising edge

FastCLK - The fast clock determines the rate at which the Fast Cluster Finder samples the input data and controls the FC1 and FC2 outputs of the chip. It is expected that this will be either 320 or 640MHz. This clock will be precisely phase shifted with BC to provide optimal operation (the phase shift is under control of the HCC chip).

RCLK - The data clock determines the rate at which data is clocked out of the chip. It is expected that this will be either 80 or 160MHz. This clock will be precisely phase shifted with BC to provide optimal operation (the phase shift is under control of the HCC chip).

BC - This is the primary clock delivered through the stave that samples the analogue channels outputs. The BC clock will be delayed by an arbitrary amount with respect to the incoming stave clock to accommodate a hybrid wide phase shift to align sensor signals with the BC.

L0_COM - This 80Mb/s signal is comprised of two time multiplexed 40Mb/s components:

L0 - A one bit BC synchronous signal signalling that data in the pipeline has been identified as an event to store into the L1Buffer. The resultant action is to transfer the data from the pipeline into the L1Buffer with a BC tag and a L0 tag generated internally.

COM - The input for the Command Decoder that will be processing commands. Commands can be received independently of the status of the triggering system and during physics data taking. The normal length of a command is 58 bits.

R3_L1 - This 80Mb/s time is comprised of two time multiplexed 40Mb/s components:

R3L0ID - The Regional Readout Request (R3L0ID) signal is delivered on one phase of the BC clock and has two fields and a length of 11 bits : 3 bits act as start bit pattern (101), followed by 8 bits containing the L0ID identifier of the event to retrieve in the L1Buffer. The idle state between consecutive R3L0ID bits is zero with at least one zero separating 2 consecutive R3L0ID.

L1LOID **-** The second trigger level (L1L0ID) signal is delivered on one phase of the BC clock and has two fields and a length of 11 bits : 3 bits act as start bit pattern (110), followed by 8 bits containing the L0ID identifier of the event to retrieve in the L1Buffer. The idle state between consecutive R3L0ID bits is zero with at least one zero separating 2 consecutive R3L0ID.

3.1.2.2 Bi-Directional Signals

The table below defines the ABC130 bidirectional signals used to transfer the data across adjacent ABC chips and the HCC.

Table 3-2 Bi Directional Data Communication Signals

Name	Type	Description
XOFFL	SLVS	Chip to Chip Data Packet Flow control
XOFFR	SLVS	Chip to Chip Data Packet Flow control
DATAL	SLVS	Chip to Chip Data Packet Input/Output
DATAR	SLVS	Chip to Chip Data Packet Input/Output

XOFFL/XOFFR - When true, the chip is not ready to receive data from the adjacent chip in the serial chain. XOFF will be controlled by a priority encoder set by the chip position number as well as data in the queue in the local ASIC. Can be set as input or output.

DATAL/DATAR - Serialized Data passing from chip to chip from chips. Can be set as input or output.

3.1.2.3 Fast Cluster Finder Signals

The table below defines the ABC130 output signals used to transfer the Fast Cluster Finder data.

Table 3-3 Bi Directional Data Communication Signals

Name	Type	Description
FC1	SLVS	FastClusterFinder output
FC2	SLVS	FastClusterFinder output

FC1/FC2 - Serialized Data carrying the Fast Cluster Finder readout signals.

3.1.3 Analogue Signal processing

The chip must contain following functions:

1. Charge integration
2. Pulse shaping
3. Amplitude discrimination. The threshold value for the amplitude discrimination is provided as a differential voltage either from internal programmable DAC.
4. Discriminated outputs are latched either in the edge sensing mode or in the level sensing mode.
5. At the start of each Beam Crossing Clock the chip samples the outputs from the discriminators and store these values in a pipeline until a decision can be made whether to keep the data.
6. Upon receipt of a L0 Trigger signal the corresponding set of values together with its neighbours are to be copied into the L0 buffer to be retain for either R3 or L1 readout.
7. The data written into the readout buffer is to be compressed before being transmitted off the chip.
8. Transmission of data from the chip will be by means of an Xon/Xoff technique where each chip ready to pass data sends a ready signal to the chip before in the readout chain.
9. The chip is required to report of internal errors that may occur, as for example :
    a) Attempt to read out data when Buffers are empty.
    b) Buffer Overflows.
10. The ABC130 incorporates a bi-directional readout that enables the system to continue operating in the event of a single chip failure.

3.1.4 Calibration and testability

Each channel has an internal Calibration Capacitor connected to its input for purposes of simulating a "hit" strip. The Calibration Capacitors are charged by an internal chopper circuit triggered by a command. A calibration enable bit is set for every channel that can be tested. The strobe and the calibration enable signals are delivered from the control circuitry. The voltage applied to the Calibration Capacitors by the chopper is determined by an internal DAC. This is intended for use during IC testing. A tuneable delay of the calibration strobe with respect to the clock phase covering at least two clock periods is provided.

3.1.5 Compatibility

The ABC130 does not retain the compatibility with the legacy pipeline triggering mode of it's predecessors because the derandomizer buffer concept is different. It should be noted that the data readout of the ABC130 uses a different technique from the token passing scheme used on the ABCD and ABCN in 250nm, and the readout protocol is also different.

3.1.6 Detector parameters

The design of the ABC130 will be optimised for performance with short strips. The post-radiation parameters of the different types of sensors, as understood presently, combined with the estimated parameters of the front end, are summarised in Table 1.

Table 3-4 : Assumed detector electrical parameters

	Endcap smallest possible (ring 1 inner) $1.4x10^{15}$	Endcap smallest baseline (ring 1) $1.4x10^{15}$	Endcap longest baseline (ring4) $1x10^{15}$	Barrel Short Strips $1.2x10^{15}$	Barrel Medium Strips $5.6x10^{14}$	Barrel Long Strips $5.6x10^{14}$
Coupling type to amplifier	AC			AC		
Readout strip implant	N			N		
Strip pitch	74.5 μm	76.9 μm	81.6 μm	74.5 μm		
Strip Length	1.0 cm	1.7 cm	5.9 cm	2.4 cm	4.8 cm	9.6 cm
Coupling capacitance to amp	20 pF	34 pF	118 pF	48 pF	98 pF	192 pF
Sensor capacitance of strip to all neighbour strips	0.74 pF	1.26 pF	4.36 pF	1.78 pF	3.55 pF	7.1 pF
Sensor capacitance of strip to backplane	0.26 pF	0.44 pF	1.54 pF	0.62 pF	1.25 pF	2.5 pF
Possible added capacitance due to gluing hybrid to sensor	0.5 pF	0.5 pF	0.5 pF	0.5 pF	0.5 pF	0.5 pF
Total Load Capacitance ~ENC_{serial} @bias 80/160uA	1-1.5 pF <400e-	1.7-2.2 pF <450e-	5.9-6.4 pF 600-700e-	2.4-2.9 pF 400-500e-	4.8-5.3 pF 550-650e-	9.6-10.1 pF 800-1200e-
Metal strip resistance	15 Ω/cm	15 Ω/cm	15 Ω/cm	15 Ω/cm	15 Ω/cm	15 Ω/cm
Bias Resistor	1.5 MΩ	1.5 MΩ	1.5 MΩ	1.5 MΩ	1.5 MΩ	1.5 MΩ
Max leakage current per strip for shot noise and shot noise estimation Strips at -15˚C / ~ENC @ 22ns	230 nA 200e-	400 nA 250e-	980 nA 400e-	470 nA 270e-	480 nA 270e-	960 nA 400e-
Collected charge (at 500 V)	10800e-	10800e-	12600e-	11600e-	15700e-	15700e-
Estimates for total noise @bias 80-160uA & max. detector leakage	450e-	520e-	720-810e-	480-570e-	610-710e-	900-1260e-
Maximum threshold assuming 50% charge division, 10% overdrive and Landau most probable/min) S/T >3.4 (present SCT assumption)	3180e-	3180e-	3700e-	3400e-	4600e-	4600e-

Maximum noise assuming 4 sigma distance to threshold	800e- (OK)	800e- (OK)	925e- (OK)	850e- (OK)	1150e- (OK)	1150e- (OK)
Proposed threshold & threshold/noise separation[1]	2800e- 7 σ	2800e- 6 σ	3125e- 4.3-3.8 σ	3125e- 6.5-5.5 σ	3125e- 5-4.4 σ	4375e- 4.8-3.5 σ
Overdrive [fC] Walk [ns]	0.1fC Walk defined for 0.55fC-10fC @0.45fC threshold Walk ~15.5ns	0.1fC Walk defined for 0.55fC-10fC @0.45fC threshold Walk ~15.5ns	0.15fC Walk defined for 0.65fC-10fC @0.5fC threshold Walk ~14ns	0.1 fC Walk defined for 0.6fC-10fC @0.5fC threshold Walk ~15.5ns	0.25 fC Walk defined for 0.75fC-10fC @0.5fC threshold Walk ~12.1ns	0.1 fC Walk defined for 0.8fC-10fC @0.7fC threshold Walk ~15.7ns

3.1.7 Front-end

3.1.7.1 Electrical Requirements:

Note that notation convention for currents used in the entire specification is "+" for current going into (sunk by) the chip and "-" for current going out of (sourced from) the chip.

3.1.7.2 Input Characteristics:

Input Signal Polarity: The front-end circuit accepts negative signals from n-type strips

Crosstalk: (via detector interstrip capacitance)

	Input MOS bias 80uA			Input MOS bias 140uA		
Strip length [cm]	2.4	4.8	9.6	2.4	4.8	9.6
Crosstalk	3%	5%	8%	2%	3%	5.5%

Input Protection: front end input is protected with non-silicided NMOS (esdnfet) thin oxide device of dimensions 80um/120nm. The width of this device is trade-off between the ESD protection robustness and the value of parasitic capacitance added by this structure. The equivalent capacitance loading the front end input for device used is around 0.4pF. The protection should stand a 1.5kV HBM (Human Body Model) event and 0.6 A TLP (Transmission Line Pulse). The TLP is defined as a current pulse with 5ns rise time and 100ns duration time. In addition to that a series resistor of 22 Ohm is used improving response to CDM (charge device model). The value is again a trade-off between protection robustness and extra noise introduced by it.

Open Inputs: Any signal input can be open without affecting performance of other channels.

3.1.7.3 Preamplifier-Shaper Characteristics

Gain at the discriminator input: 95 mV/fC for the nominal bias currents and the nominal process parameters

Effective gain extracted from the response curve:

[1] In principle no threshold below 0.5fC is proposed (0.5fC equivalent to 45mV (DAC set to 10011), but unknown effect of digital noise, quality of powers supply and matching) except two cases for smallest Endcap detectors (threshold 0.45fC)

90 mV/fC for the nominal bias currents and the nominal process parameters

Linearity: better than 5% in the range 0 – -4 fC

better than 15% in the range 0 – -8 fC

Peaking time: 20 ns

Intrinsic peaking time of 20 ns of the circuit ensures a peaking time below 25 ns including the effect of charge collection time.

Noise: See Table 1 for maximum RMS noise allowable on fully populated modules after irradiation. Noise measured on prototype is much lower than this.

Gain Sensitivity to analogue supply voltage for 1 fC signal: < 1%/100mV

Power Supply Rejection Ratio at:

(not design targets but simulation results of the circuit)

	Input MOS bias 80uA			Input MOS bias 160uA		
Strip length [cm]	2.4	4.8	9.6	2.4	4.8	9.6
10Hz-10kHz	57dB	57dB	57dB	57dB	57dB	57dB
10kHz-1MHz	17dB	16dB	15dB	17dB	16.5dB	16dB
1MHz-10MHz	6dB	5dB	4dB	6dB	6dB	5dB
10MHz-100MHz	3dB	2dB	1dB	3.5dB	3dB	2dB

Comparator Stage:

A threshold is applied as a differential voltage offset to the comparator stage. This threshold voltage is applied from an internal 8-bit DAC (bits **BVT<0:7>**).

Threshold setting range: 0V to -590mV, nominal setting at -90mV (-1fC) before irradiation and as low as -45mV (-0.5 fC) after full dose.

Test MUX output: TEST_THDAC MIN/MAX = 2mV/133mV

Threshold setting step without trimming: 2.3mV (8-bit resolution)

Threshold spread before trimming < 15 mV RMS

The range of 5 bit trim DACs inside the channel is controllable with 5-bit DAC (bits **BTRANGE<0:4>**).

TrimDAC threshold setting range MIN/MID/MAX 50mV/150mV/255mV (controllable with 5 bit DAC)

TrimDAC resolution MIN/MID/MAX 5 bit (step 1.55mV/5mV/8mV)

TEST_TRDAC MIN/MID/MAX 36mV /95mV/150mV

3.1.7.4 Timing Requirements:

Time walk: ≤ 16 ns.

This specification depends on the precision of the digital acquisition latch edge. Good alignment, 1 or 2 ns over a common clocked array of channels implies a longer time walk assignment to the rising edge of the shaped signal.

Time walk defined:

For non-irradiated detectors; the maximum time variation in the crossing of the time stamp threshold over a signal range of -0.75 to -10 fC, with the comparator threshold set to -0.5 fC; For non-irradiated detectors time walk is in the range of **12.5ns**

For different cases of irradiated detectors please refer to Table 3-4

Double Pulse Resolution: ≤ 75 ns for a -3.5 fC signal followed by a -3.5 fC signal at -0.5fC threshold

Max recovery time for a -3.5 fC signal following -80 fC signal: 200ns

3.1.7.5 Calibration circuit

Calibration signal distributed with one calibration line can be applied to on-chip calibration capacitor (60fF) connected to front end input with CMOS switch controlled with one of the channel configuration bit. Address and the number of connected channels to the calibration line, as well as the amplitude of the calibration signal and its delay is set via the control logic.. The voltage applied to the Calibration Capacitors by the chopper is determined by an internal 8-bit DAC. The calibration line is also brought through analog test mux to pad where the calibration voltage can be directly measured during the screening of the chip (analog test mux address 12).

A tuneable delay of the calibration strobe with respect to the clock phase covering at least two clock periods is provided. The delay is built in chain of delay cells designed with current starved inverters and it is controlled with 6-bit register (bits **STR_DEL<0:5>**). The absolute delay magnitude is obtained by the calibration delay scans using known BCO period with high input signals and low discriminator threshold. In order to compensate for the process variation a 2 bit register to set the range of the strobe delay is provided (bits **STR_DEL_RANGE<0:1>**). For nominal corner of the technology process, the following delays of the calibration strobe can be obtained:

STR_DEL_RANGE =00	strobe disabled
STR_DEL_RANGE =01	delay 0 to 50ns
STR_DEL_RANGE =10	delay 0 to 60ns
STR_DEL_RANGE =11	delay 0 to 80ns

Calibration Capacitors: 60 fF ±10% (3 sigma) over full production skew, ±1% (3 sigma) within one chip.

Calibration signal:

amplitude range: 0 – 150 mV (charge range: 0 – 9 fC)

amplitude step: 0.586 mV (charge step: 0.035 fC)

Absolute accuracy of amplitude: to be calibrated during chip preselection.

Calibration DAC is controlled through bits **BCAL<0:7>** of the control registers.

3.1.7.6 Biasing circuitry and output test multiplexer

The preamplifier input transistor and feedback bias currents are controlled by the internal 5-bit DAC converters referenced to the internal bandgap circuit. The predicted variation of the bandgap reference is of the order of +/- 40mV pk-pk over 592mV nominal valu

e. In order to compensate for the variations of the bandgap reference voltage as well as for the variation of the resistors setting the bias currents, the internal bias reference generators can be calibrated with 5-bit DACs.

To adjust internal bias for voltages VCS, VCD, VCSP, VBASE and VB one should set bits **BVREF<0:4>.** For nominal technology parameters BVREF=01101[1] should give TEST_VR =50mV (nominal).

To adjust internal bias for bias current generators (IPRE, IFEED, and many others internal currents) one should set bits **BIREF<0:4>**. For nominal technology parameters BIREF=01101 should give TEST_IR =50mV (nominal).

To adjust internal bias for 8-bit threshold and calibration DACs one should set bits **B8BREF<0:4>**. For nominal technology parameters B8BREF=01101 should give TEST_R8B =50mV (nominal).

Two bias currents can be set to the desired operating point;

IPRE (preamplifier input transistor bias), register bits: **BIPRE<0:4>**

Nominal value (half DAC range - 10000): 110uA

MIN/MAX (00000/11111): 80uA/140uA

Test MUX output: TEST_IPRE MIN/NOM/MAX = 90mV/123mV/155mV

IFEED (preamplifier feedback transistor bias), register bits: **BIFEED<0:4>**

Nominal value (MSB-LSB 01001): 300nA

MIN/MAX (00000/11111): 160nA/600nA

Test MUX output: TEST_IFEED MIN/NOM/MAX = 16mV/30mV/65mV

ICOM (comparator bias), register bits: **BICOM<0:4>**

Nominal value (MSB-LSB 10000): 9uA

MIN/MAX (00000/11111): 5uA/13uA

Test output (activated by bit control BTMUXD):

TESTCOM MIN/NOM/MAX = 20mV/36.5mV/52mV

3.1.7.7 Test multiplexer

For testing purposes the front end block is equipped with analog test multiplexer which is controlled through configuration registers. It connects the test points located in the bias block through switches to common line connected to the output pad.

Analog test MUX:

Address 0 → TEST_TRDAC

Address 1 → TEST_VR (nominal value =50mV → to be adjusted with **BVREF<0:4>**)

Address 2 → TEST_IR (nominal value =50mV → to be adjusted with **BIREF<0:4>**)

Address 3 → TEST_R8B (nominal value =50mV → to be adjusted with **B8BREF<0:4>**)

Address 4 → TEST_IPRE

Address 5 → TEST_IFEED

Address 6 → VCS (VCS bias voltage → nominal value 900mV)

Address 7 → VCD (VCD bias voltage → nominal value 600mV)

Address 8 → VCSP (VCSP bias voltage → nominal value 600mV)

Address 9 → VBASE (VBASE bias voltage → nominal value 500mV)

Address 10 → VB (VB bias voltage → nominal value 450mV)

[1] In all cases bits given in the order <MSB…LSB>

Address 11 → VBG (bandgap voltage → nominal value 592mV)

Address 12 →CALLINE (calibration line)

Address 13 → TEST_THDAC (test point of the threshold DAC)

The access to the analog multiplexer is through the passive analog pad AMUXOUT. The access to the test point of the DAC used for bias of the discriminator (supplied with digital power domain) is at the pad TESTCOM.

3.1.8 Channel Order and Channel Numbering

Channels identification in data packets are using numbers 0 to 127 attributed to "one row" of a strip detector (barrel like geometry) and numbers 128 to 255 to "another row" of the detector.

Therefore 134 and 135 are adjacent strips of the second row, 254 is the last but one strip of the second row while 1 is the second strip of the first row (128 can not be adjacent to 127 …).

The arrangement of the wire bonds from the detector to the input pads of the front-end channels is reported here for the barrel case.

The order in which the front-end channels are physically placed and connected to the detector strips is described in the Table 3-5 :

ABC channel number (0 to 255) in data packet	FE channel order number (from 0 to 255) in configuration and setting registers	Detector strips row (2 rows with strips 0 to 127, row 1 and row2)
0	0	0 in row1
1	1	1 in row1
128	2	0 in row2
129	3	1 in row2
..	..	..
126	252	126 in row1
127	253	127 in row1
254	254	126 in row2
255	255	127 in row2

Table 3-5: Channel numbering convention

3.1.9 Input Register and Mask Register

The functions of the input register and mask register will be implemented in a single functional block.

3.1.9.1 Input Register

This register latches the incoming data with the rising edge of BC, delivering a clocked pulse to the pipeline (L0buffer).

3.1.9.2 Edge Detection Circuitry (actually not implemented in ABC130)

The function of this block is to detect a low to high transition in the data entering the pipeline, and for each of such transition found the circuit generates a pulse of duration 1 clock cycle irrespective of the length of the incoming pulse. The effect of this block is that only a single '1' is written into the pipeline for every hit detected regardless of the response time of the discriminator. This circuitry can be turned on or off by setting the appropriate bit in the configuration register.

3.1.9.3 Channel Mask Register

This register serves a dual purpose. Firstly, the Channel Mask register enables any bad or noisy channels to be turned off thus preventing them from increasing the data rate due to false hits. Secondly, it can be used during chip testing to apply a set of test patterns to the pipeline. In the test mode the test pattern appears at the input of the pipeline. In Mask mode, a channel is masked with '1'. In Test mode, a channel gets the Mask bit value. The 256 bits Channel Mask register is built as 8 registers of 32 bits, each one being addressable in write or read by Control Commands (addresses $10 to $17). The masking bits order is from register $10 (channels 0 to 31) to $17 (channels 224 to 255), with the channels numbered as the front-end order (column 2 of Table 3-5).

Table 3-6 : Masking Register Modes of Operation

TM bit	Mode of Operation
0	Normal Data Taking (Contents of register used to "Mask Inputs")
1	Test Mode (Contents of mask register are used to supply test values to pipeline)

3.1.9.4 Input Pattern Register

This register serves as signal pattern monitor at the pipeline input. The 256 bits Pattern Input register is built as 8 registers of 32 bits, each one being addressable in write or read by Control Commands (addresses $18 to $1F). The bits order is from register $18 (channels 0 to 31) to $1F (channels 224 to 255), with the channels numbered as the front-end order (column 2 of Table 3-5).

3.1.10 FAST CLUSTER FINDER (ABC130_1 version only)

The Fast Cluster block is a prototyping block included on the ABC130 that, when enabled, will provide prompt, beam clock synchronous, cluster position data to an external device that will correlate clusters between tracking layers and select high PT coincidences to send to the Trigger processor. The fast cluster algorithm assumes that the ABC130 is bonded with the two rows of strips interleaved as described in 3.1.8. Strip data is provided from the input of the ABC130 pipeline after the mask register. This allows noisy channels to be masked off to avoid having a cluster registered at most or all beam crossings from improperly functional channels. Data from these banks are processed independently and in parallel of the other ABC functions. They are driven by the FastCLK clock signal.

Its block diagram is shown on Figure 3-2 and its main feature are:

- Parallel processing of cluster finding from each 128 strip bank
- One dedicated High Speed Serialized output per bank of 128 strips (2 per ABC130)
- Rejection of Low momentum tracks by limiting the number of hit strips in a cluster to 2
- Half Strip Precision achieved by listing how many strips were hit (1 or 2)
- Fixed Delay from BC - Serialized data will be sent with a fixed delay from cluster's BC :
  5 BC delay with a 160 MHz Serializing Clock
  2 BC, dead timeless, delay with a 640 MHz clock
- Power (when enabled) with Drivers
- Logic + Serializer 4.5 mW + 9 mW for two Drivers @160 MHz
- Logic + Serializer 5.5 mW + 12 mW for two Drivers + 3 mW for receiver @ 640 MHz

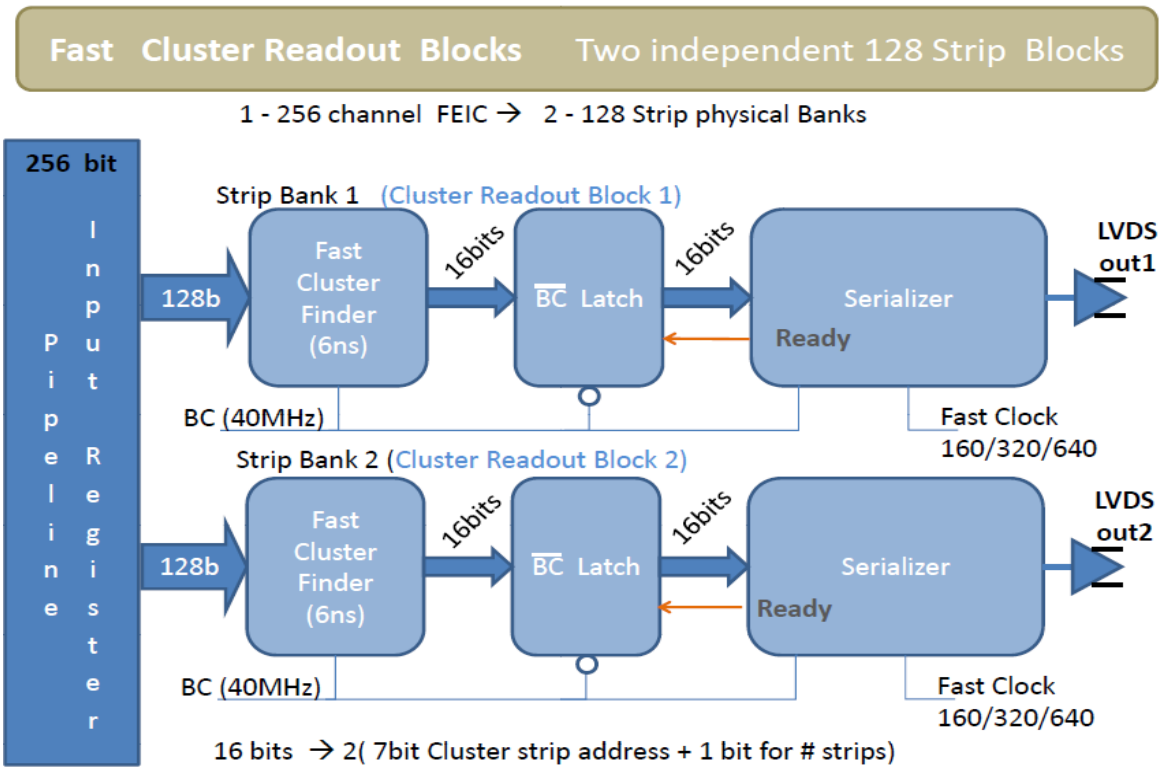


Figure 3-2: Block diagram of the fast cluster blocks in ABC130

Fresh strip data is loaded into the pipeline at the rising edge of the BC. This data (odd channels to one cluster finder and even channels to the other) is evaluated using combinatorial logic in 6 ns. The Cluster Finder output consists of two 8-bit words for each bank, where the 8-bit word represents a 7-bit address plus one bit to indicate the number of hit strips (1 or 2). Given the 80 μm strip pitch for the upgraded strip detector this will effectively yield a phi resolution of 40 μm. In the event that fewer than two clusters are found, the output 8 bits are set to an illegal combination, all 1's. A latch on the negative edge of BC will record the Cluster Finder data if the serializer is ready. The serializer will start on the next rising edge of the BC clock. When serialized at 640Mbps, the 16 bits of cluster data is sent to the outputs FC1 and FC2 every BC period within a 2 BC period delay and no cluster finder data will be lost. Figure 3-3 shows a timing diagram of this process. In the event of more than two qualifying clusters in a single BC, the two clusters nearest the edges of the bank (lowest and highest addresses) are sent out and clusters between these are lost.

A special framing mode is provided when a bit is set by the command decoder. In this mode the serializer outputs send 8 1's followed by 8 zeros to establish the data frame according to the local clocks.

Complementary information is given below:

1) Referring to the Pipeline input register, the fast cluster finder differentiates between banks of strips according to type "odd" or "even". Our addressing scheme starts with 0: (bank 1 has Strips 0 2 4 6 ... bank 2 Strips 1 3 5 7....) (We need to check that the wiring to the pipeline register is consistent with this scheme).

There should be no problem with reversal of the order due to the two possible chip orientations versus strips in a hybrid design.

2) Each bank of 128 strips has one cluster finder block. (Two cluster finder blocks per ABC130)

3) Cluster finding proceeds from both ends of each bank towards the middle. A cluster is defined as not more than two consecutive hit strips.

4) A recorded cluster is represented by a 7 bits address plus 1 bit to indicate the number of strips over threshold. 8 bits / serialized cluster

5) Up to two clusters per bank (16 bits) may be sent to the serializer. The highest address number will be serialized first. (4 clusters/BC from one ABC130)

In the event that one or both clusters are missing the corresponding serialized (8) bits will be filled FF. Thus an evaluated BC with no clusters will result in FFFF being sent.

6) If more than two clusters are detected by a cluster finder a 16 bit counter will be incremented. Two cluster finders --> 2 counters --> 32 bits word. The counter value is read by a STATUS read command at address $33.

7) Each serializer sends a fixed length word of 16 bits on the outputs FC1 or FC2 for each evaluated BC. If a 640MHz FASTClock is used, a 16 bits word can be sent within each beam crossing period. Data will be sent with a fixed 2 BC latency.

8) Framing: to detect the serializers phase at the ABC130 FC1 and FC2 outputs, a special mode of operation will be enabled. The 16 bits of the serializers will be low for the first 8 bits and high for the second 8 bits of each 16 serialized bits word.

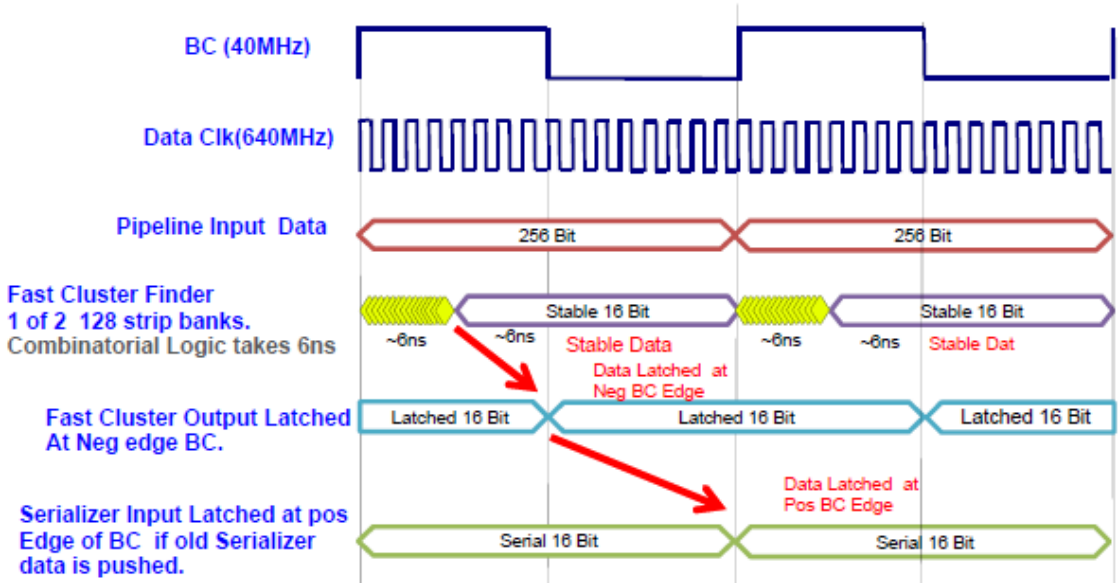


Figure 3-3: Cluster finding Logic Data synchronization. Data Latched at the serializer input (bottom trace) is immediately sent out serially.

3.1.11 L0BUFFER (Pipeline)

The binary pipeline L0BUFFER is realised with two single port RAM blocks of 320 bits (wide) by 128 bits (length). The total pipeline length is 256 bits, or 6.7us latency time. Out of the 320 inputs, 256 are for the hit data, 8 are receiving the BC counter data, and the remaining will be unused (zeroed) or used for Error Recovery Code. When a L0 trigger is received (L0_COM input), the hit-pattern and BC count from the three time bins written in the pipeline at a predefined number (LAT) of clock cycles before are readout and transmitted to the L1BUFFER. LAT is the number of clock cycles representing the L0 delay time. The value of LAT is programmable through the command decoder and stored in an internal register (LAT Register). With a command "reset" the clock generator is reset while the contents of the pipeline remains unchanged. A description of the L0Buffer arrangement is shown in Figure 3-4.

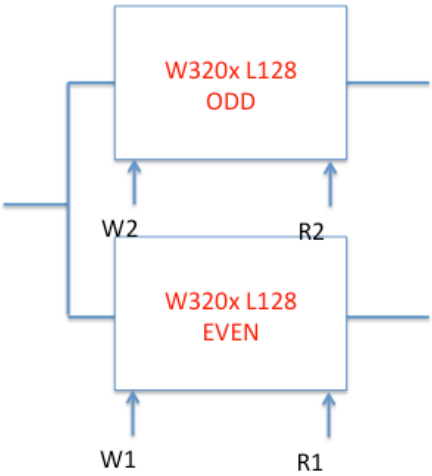


Figure 3-4 L0Buffer (pipeline) arrangement in 2 blocks of 128 320-bits wide words.

The physical array size of the L0BUFFER will be 320bits word width by 256 bits length (82Kbits), because of the RAM block design constraints. The additional word bits can be used to add Hamming code correction bits. 32 bits may be enough to correct one bit flip across the significant 256 bits of a word. One may choose to correct only the 8 bits of the BC counter. Calculations in note 3-1-A are given to estimate the probability of bit flip in the L0BUFFER.

Note 3-1-A : Estimate of SEU error probability in the L0BUFFER block :

Bit flip cross section : 1E-14/cm2

Particle hit rate in LHC environment at 5*10E34 (extrapolated from numbers at 1*10E34, pre H-LHC simulations) : 5 times 1.2E13/cm2.year of run (only simulation safety factor applied), at 35 cm radius.

One run year time (6 months run) 15E6 seconds

Hit rate per second : 4.0E6/cm2.s

Bit flip 4E-8 per second per bit

Probability of one bit flip per 25E6 seconds (289 days) per bit

In 6.7us : probability of bit flip per bit : 2.7E-13

For 82Kbits memory : probability of one bit flip per 300 seconds per memory

In 6.7us : probability of one bit flip within 82K : 2.2E-8

From these numbers it appears that the physics data bit error rate will be 1 bit error per 300 seconds, ie per 15E6 packets transmitted (a bit error translates in a false cluster position or false hit bit)

Considering only the 8 BCID bits for event identification the rate is reduced to one bit flip per 12000 seconds per chip, ie per 600E6 packets transmitted (a BCID bit error translates into a false packet-to-event identification). The system has ~300K ABC chips, then there will be one packet badly identified every 0.4s or every 20K L1 events transmission (it is a worst case as chips will not all receive the same amount of particles).

3.1.12 L1BUFFER

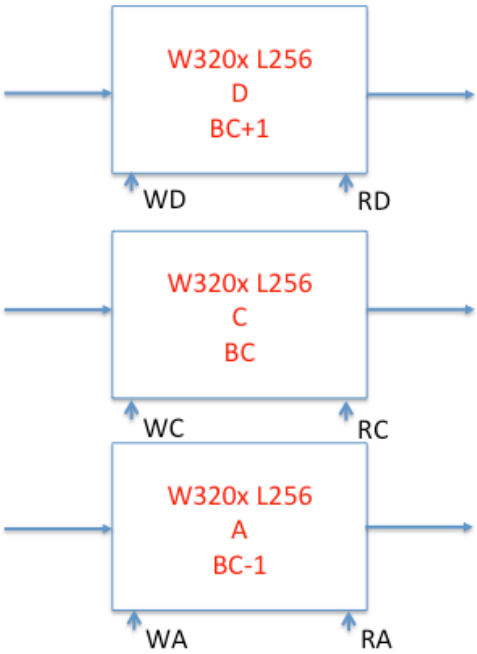


Figure 3-5 L1Buffer arrangement in 3 blocks of 256 320-bits wide words.

The readout buffer L1BUFFER is realised by three single port RAM blocks of 320 bits (wide) by 256 bits (length) (246Kbits in total). The buffer length is able to store 256 L0 tagged “events”, one event being made of the records of the hits for 3 consecutive time slots: the time slot before (BC-1), the one tagged by L0 (BC), and the one after (BC+1). With an average L0 event readout rate of 500KHz, the events are stored in the L1BUFFER for an average duration of 512 microseconds. Out of the 272 inputs, 256 are for the hit data, 8 are for the BC counter data, 8 are for the Local_L0ID data (see XXX paragraph for the definition of Local_L0ID).

The additional word bits can be used to add Hamming code correction bits. 32 bits may be enough to correct one bit flip across the significant 272 bits of a word. One may choose to correct only the 16 bits of the BC counter and Local_L0ID, as these numbers are critical for the event identification. Calculations in note 3-1-B are given to estimate the probability of bit flip in the L1BUFFER.

Note 3-1-B : Estimate of SEU error probability in the L1BUFFER block :

Bit flip cross section : 1E-14/cm2

Particle hit rate in LHC environment at 5*10E34 (extrapolated from numbers at 1*10E34, pre H-LHC simulations) : 5 times 1.2E13/cm2.year of run (only simulation safety factor applied), at 35 cm radius.

One run year time (6 months run) 15E6 seconds

Hit rate per second : 4.0E6/cm2.s

Bit flip 4E-8 per second per bit

Probability of one bit flip per 25E6 seconds (289 days) per bit

In 5ms : probability of bit flip per bit : 2E-10

For 250Kbits memory : probability of one bit flip per 100 seconds per memory

In 5ms : probability of one bit flip within 250K : 5E-5

From these numbers it appears that the physics data bit error rate will be 1 bit error per 100 seconds, ie per 5E6 packets transmitted (a bit error translates in a false cluster position or false hit bit).

Considering only the 16 bits for event identification (L0NUM and BCID) the rate is reduced to one bit flip per 2000 seconds (34 mn) per chip, ie per 100E6 packets transmitted (a ID bit error translates into a false packet-to-event identification). The system has ~300K ABC chips, then there will be one packet badly identified every 66 ms or every 3300 L1 events transmission (it is a worst case as chips will not all receive the same amount of particles).

L1BUFFER Readout mechanism

The ABC130 allows a multi-trigger data flow control retaining the Beam Crossing synchronous pipeline transfer signal (L0 here) from previous versions, a new asynchronous Regional Readout Request (R3) and a second level asynchronous data readout intended for a global readout (L1).

Definitions of terms:

L0: “zero” level trigger signal, broadcast to all chips, at fixed latency after the event (L0-L1 chip input)

R3: signal addressed to a fraction (10%) of the detector, requests the readout of events tagged by a number “R3L0ID”, 8bits streamed just after the R3 signal on the R3s chip input.

R3L0ID: 8bits used to identify the event to readout attached to an R3 command.

L1: signal addressed to the full detector, requests the readout of events tagged by a number “L1L0ID”, 8bits streamed just after the L1 signal on the L0-L1 chip input.

L1L0ID: 8bits used to identify the event to readout attached to an L1 command.

The L1BUFFER operation is rather simple to explain: at every occurrence of L0, one event of the L0BUFFER is written in L1BUFFER (3 BC slots). At any occurrence of R3 or L1, one event is read out (3 BC slots) and sent to the Data Compression Logic blocks (one specific for R3, one specific for L1).

The identification of the event to readout, within the L1BUFFER memory array, is made with the R3L0ID (L1L0ID) numbers: these numbers are used as direct pointers (address generators) for reading the L1BUFFER. If R3L0ID and L1L0ID have the same value, they read the same event.

To correctly address the event to readout, with values of R3L0ID (L1L0ID), the event has to have been written, at L0 time, at locations pointed with an internal address generator, called Local_L0ID. Local_L0ID is incremented by one at each L0 reception, and initialized to zero at the same time that the EXTERNAL values R3L0ID and L1L0ID are initialized to zero.

A typical sequence of signals to operate the data extraction from the L0BUFFER and L1BUFFER is shown on Figure 3-7.

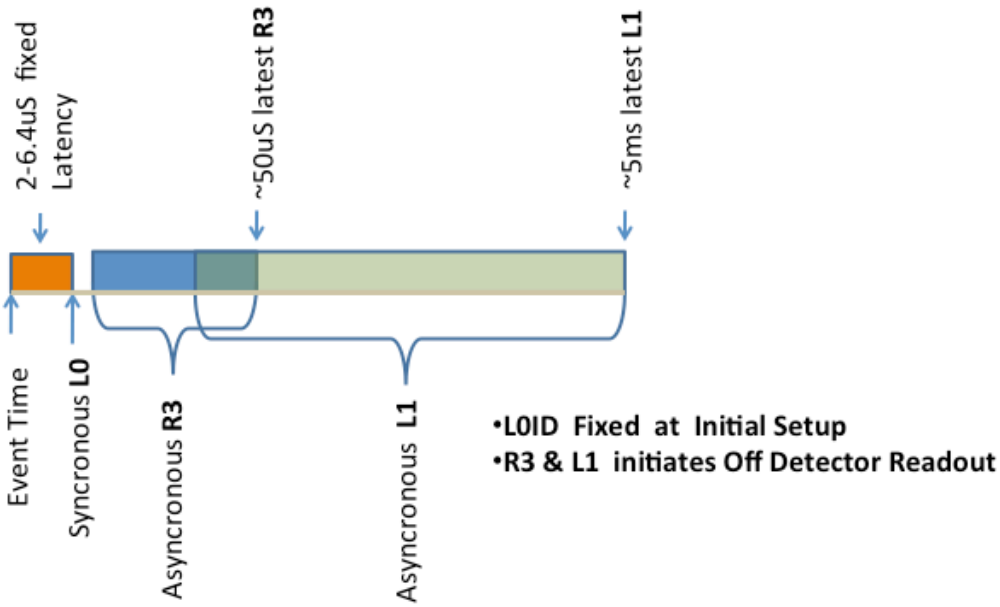


Figure 3-6: L0, R3 and L1 Latencies

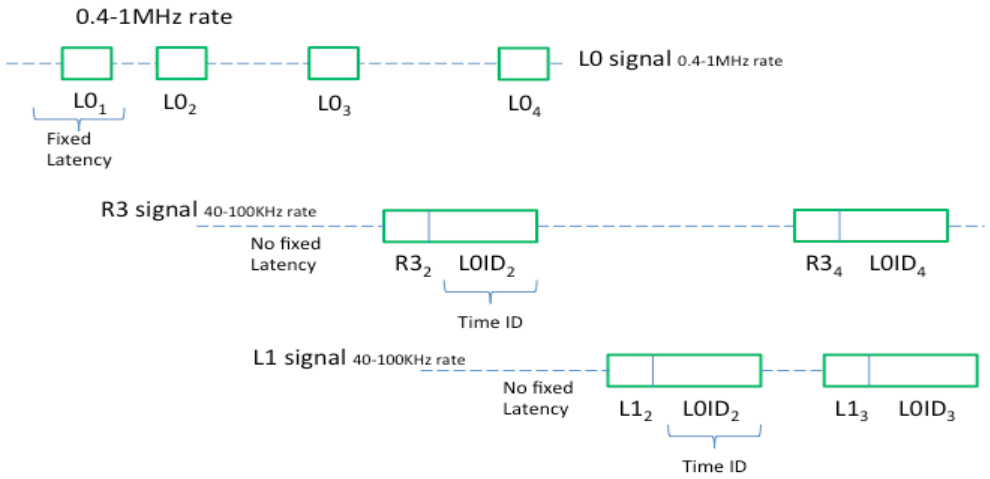


Figure 3-7: Sequence of L0, R3, L1 signals used to trigger the physics data readout.

3.1.13 Data compression logic for L1 readout

It is anticipated that on any event a limited number of channels will contain hits. This fact can be used to reduce the number of bits of data that have to be read out of the chip for each event. The data compression logic works by examining in turn the 3 bits of data in 3 consecutive bunch crossings that make up the hit pattern for each channel. Each group of 3 bits is compared against one of 4 selectable criteria. If the pattern meets the criteria, then two cases:

1- The channel address (8 bits) is created and the criteria is applied to the three consecutive channels, adding 3 more bits: "0" if the criteria is not met or "1" in the opposite case. The total of 11 bits about 4 consecutive channels form a L1-1BC cluster. Then the process is repeated from the first channel after the last one in a cluster until the hit patterns of the two groups of 128 channels have been scanned.

2- The channel address is created, the 3 bits for bunch crossing of data is made available, together with the 3 bits of the 3 next channels in the row. The total of 20 bits about 4 consecutive channels form a L1-3BC cluster. Then the process is repeated from the first channel after the last one in a cluster until the hit patterns of the two groups of 128 channels have been examined.

The condition for case 1 or 2 will depend on the status of a OR of 2 control bit (control bits to be defined)

The following table shows the 4 selection criteria (currently there are only plans to use 3, the 4th is for chip testing only).

mode(1:0)	Name of Selection Criteria	Hit Pattern (Oldest data bit 1st)	Usage
00	Hit	1XX or X1X or XX1	Detector alignment
01	Level	X1X	Normal Data Taking
10	Edge	01X	Normal Data Taking
11	Test	XXX	Test Mode

Table 3-7 : Data Compression Criteria. X = Don't care state

Name	**I/O**	**Function**
clock	input	40MHz clock
rst_b	input	active low reset
mode[2 :0]	input	3bit defining the data compression criteria
mcluster	input	when high DCL is looking for 3 clusters/packet
nbpacket[?:0]	input	bit giving the maximum number packet per event
ask_data	output	one clock pulse asking the next event to process
buffwr	input	3 clocks pulses writing the event to process
datain[255 :0]	input	one BC 256bit data (event)
datain[271:256]	input	16bit event's L0ID and BCID
packet[50:0]	output	packet result
fifo_full	input	when high the packet fifo is full
fifowr	output	one clock pulse writing packet in the packet fifo

Table 3-8 : L1 Data Compression Logic Input/Output Signal Definitions (ABC130)

Packet bits are ordered as :

Packet[50:35]	Packet[34:33]	Packet[32:35]
Field 1	Field 2	Field 3
BCID and L0ID	Empty flag(ep), Last Flag(lp)	33 bits compression result

Table 3-9 : Packets Field definition at output of L1-DCL

- The field 1 (packet[50:35]) contains the 16 bits of L0ID and BCID that are readout from the L1BUFFER at the L1 event readout.
- The field 2 (packet[34:33]) contains 2 bits which will be part of the TYP definition of the packet : the “ep” bit indicates that the chip has no cluster. The “lp” bit indicates that the last cluster has been found. Both bits can be used as indicators to not wait for another packet out of that chip for the L1L0ID tagged event.
- The field 3 (packet[32:0]) contains 1, 2 or 3 clusters of 11 bits (L1-1BC clusters) : in case of a chip having only one or two clusters to be readout in the packet, the last cluster data is repeated in the empty part of the packet.

  or

- The field 3 (packet[32:0]) contains one L1-3BC cluster (20 bits) followed by 13 undefined bits.

Format description packet[32:0]

L1-3BC packet: (1 cluster when mcluster = 0)

ch0[7:0], hit0[2:0], hit1[2:0], hit2[2:0], hit3[2:0], tbd[12:0] = 33 bit

L1-1BC packet: (3 clusters when mcluster = 1)

ch0[7:0], nxthit0[2:0], ch1[7:0], nxthit1[2:0], ch2[7:0], nxthit2[2:0] = 33 bit

Remarks

If a packet contains lp=1 (packet[33]) , it means it is the last packet of the current event.

If a packet contains ep=1 (packet[34]), it means this event is empty.

This block operates as follows.

After the chip receives a L1 trigger, if it is not already processing data, or in a condition that prevents the readout process, the L1BUFFER is read and three 256-bit words that are the event bits are copied from the L1BUFFER into the L1-DCL. At the same time the 16 bits containing the values of BCID and L0ID are copied to an internal register.

The 3 times 256 bits are separated in 2 blocks of 3 times 128 bits-registers at the L1-DCL input, to group together bits of adjacent channels in a strips row : one block treats “odd” numbered channels, the other one treats “even” numbered channels.

The data compression logic then starts to scan through the bits of the 3 times 128 bits-registers simultaneously in the 2 blocks, until it finds one channel which has a pattern of hits which matches the data selection criteria. If it finds such a pattern of hits, it creates the 8 bits address of the channel. It applies the same data selection criteria to the 3 next channels, and creates 3 bits of matching. The logic then continues scanning channels through the 2 “odd” or “even” blocks up to the next channel that matches conditions:

- If one is found, then a second “L1-1BC cluster” word of 11 bits is created
- If another one is found, then a third “L1-1BC cluster” word of 11 bits is created, at which point the 33 bits of Field 3 are filled, and a signal is sent to write the L1-DCL packet outputs into the Readout Block FIFO.
- In case of a second or third one are not found when reaching the last channel in both the “odd” and “even channels” blocks, then the “lp” bit is set, the Field 3 is filled with copies of the last “1BC-cluster” information, and a signal is sent to write the L1-DCL packet outputs into the Readout Block FIFO.
- In case the last channel in both the “odd” and “even channels” blocks is not reached after finding 3 1BC-cluster, the scan process is restarted after the write to the Readout Block FIFO is done, and a second packet is build with the same rules as the first one (ie : copy of last L1-1BC cluster if less than 3 clusters detected, lp bit set if last channel reached, continues the channels scan through building more packets until channel 128 in the “even channels” is reached).
- If no channel was found to match the data selection criteria, then the packet is formed with undetermined bits in Field3 and the bit “ep” is set to one (empty packet).

3.1.14 Data compression logic for R3 readout

3.1.14.1 R3 DCL Operation

Pin Name	Function		Direction
CLK	40 MHz Clock		Input
rst_b	System reset	Active low	Input
data_in [271:0]	data_in [271:256] = L0 and BC ID (16 bits) data_in [255:0] = Single event (256 bits)		Input
buffwr	A clock width pulse to write the event data to the DCL buffer	Active high	Input
FIFO_full	Indicates if the FIFO which the DCL is writing to is full.	Active high	Input
EN_01	Enables the zero-to-one detection functionality in the DCL.	Active high	Input
wtdg_rst_b	Similar to rst_b but controlled by the watchdog counter.	Active low	Input
FIFO_wr	A clock width pulse used to transfer the DCL packet to the FIFO. This is high when the DCL packet is ready.	Active high	Output

busy	High when the DCL is not in the idle state.	Active high	Output
wtdg_rstrt	Restarts the watchdog counter. High when the DCL is busy or FIFO is full.	Active high	Output
PCKT_o [50:0]	51 bit packet. PCKT_o [50:35] = L0 and BC ID. PCKT_o [34:27] = Position of 1st hit PCKT_o [26:19] = Position of 2nd hit PCKT_o [18:11] = Position of 3rd hit PCKT_o [10:3] = Position of 4th hit PCKT_o [2] = 01 Detection flag PCKT_o [1] = Overflow flag PCKT_o [0] = Not empty flag		Output

Table 3-10: R3-DCL I/O Pin Description

The DCL is expected to read event data from silicon strips made up of 256 channels. The DCL would detect the different positions of hits in the event and report it in a packet. It only recognizes the hits with cluster width less than 3 channels wide up to a maximum of 4 hits per event. All other hits would be discarded.

From the input, the DCL processes every third event. If the zero-to-one detection is enabled then another filtering process would be applied which would make the DCL only process the events with zero-to-one transition in any of the channels between the second and third event.

To the output, the DCL would produce a packet which has the L0/BC ID of the event, positions of a maximum of 4 detected hits and three bit flags. The first flag showing whether there has been a zero-to-one transition detected (used to discriminate between a packet of an empty event and that of a discarded event due to the zero-to-one filtering process). The second showing if there were more than 4 hits in the event. And last but not least, the Not-empty flag which is used to show whether the event had any hit.

3.1.14.2 Zero to one detector

The DCL expects three buffwr pulses (1 pulse with 3 clock pulse width). It reads in the first two events and ignores the last. When the zero to one detection is enabled (EN 01 = 1) the zero to one detector would signal the rest of the blocks to perform the hit locating, cluster identification etc. on the 2rd event data, if there was at least a single zero in the 1st event that turns into a one in the 2nd. If the zero to one detection is disabled (EN 01 = 0) the DCL will always process the 2nd event data. The data input is 272 bits wide. The first 16 bits are the L0BCID and the rest 256 bits are the strip data. The L0BCID are not included in the zero to one detection but are brought forward with the strip data.

EN_01=1:

Sending for instance

(256'h8000000000000000000000000000000100000000000000000000000000000001)

Throughout the 3 buffwr pulses would not trigger the DCL and an empty packet would be produced.

Sending

(256'h0000000000000000000000000000000000000000000000000000000000000000)
(256'h0000000000000000000000000000000000000000000000000000000000000000)
(256'h8000000000000000000000000000000100000000000000000000000000000001)

With a single buffwr pulse would produce a packet reporting the hit locations of the last event. If we assumed that the first event has a BCID of 92, second 93 and third 94, then 94 would be reported along with the hit locations.

For example EN_01=0

No matter what is sent throughout the 3 buffwr pulses the second is always processed.

Sending the same event data as the examples above (sending different and identical events) would result with the same output.

3.1.14.3 Cluster Identification

The R3 DCL reports any hit with a cluster width < 4. It reports the location of the first 1 for clusters with width of 1 or 2 and reports the location of the central strip when the cluster width is 3.

3.1.14.4 Hit locating

The DCL now deals with the strip data as odds and evens. It processes the first 128 bits of odd bits followed by the other 128 even bits. The DCL reports a maximum of 4 hits per event.

With reference to the simulation test bench, the DCL will report the positions of example hits as follows:

‘TB.DataFieldRow1 = 128’h80000000000000000000000000000000;
‘TB.DataFieldRow2 = 128’h00000000000000000000000000000000;

This would report 127,0,0,0.

‘TB.DataFieldRow1 = 128’h80000000000000000000000000000001;
‘TB.DataFieldRow2 = 128’h00000000000000000000000000000000;

This would report 0, 127, 0, 0.

‘TB.DataFieldRow1 = 128’h80000000000000000000000000000001;
‘TB.DataFieldRow2 = 128’h80000000000000000000000000000000;

This would report 0, 127, 255, 0.

‘TB.DataFieldRow1 = 128’h80000000000000000000000000000001;
‘TB.DataFieldRow2 = 128’h80000000000000000000000000000001;

This would report 0,127,128,255.

3.1.14.5 Packet construction

The DCL constructs a 51 bit packet containing the following:

|L0ID|BCID|Hit 1|Hit 2|Hit 3|Hit 4|No 01|Overflow|Not empty|

8 bits: L0ID, BCID, Hit 1,2,3 and 4.

1 bit: No 01 (1 when 01 detection is enabled and no 01 change is detected), Overflow (1 when more than 4 hits exist in the event) and Not empty (1 when at least 1 hit is reported).

3.1.15 Readout Circuitry

clk	I	clock signal 80/160MHz
bclk	I	beam(bunch) clock 40MHz
rstb	I	reset, active low
ID[6:0]	I	chip ID
priority[3:0]	I	priority on the chip-to-chip serial chain from control logic
dir	I	chip-to-chip direction control from command/control logic
DATLoen	O	chip-to-chip serial chain left-side data driver output enable active low
DATRoen	O	chip-to-chip serial chain right-side data driver output enable active low
XOFFLoen	O	chip-to-chip serial chain left-side flow-control driver output enable active low
XOFFRoen	O	chip-to-chip serial chain right-side flow-control driver output enable active low
DATLi	I	chip-to-chip serial chain left-side data input
DATRi	I	chip-to-chip serial chain right-side data input
XOFFLi	I	chip-to-chip serial chain left-side flow-control input
XOFFRi	I	chip-to-chip serial chain right-side flow-control input
DATLo	O	chip-to-chip serial chain left-side data output
DATRo	O	chip-to-chip serial chain right-side data output
XOFFLo	O	chip-to-chip serial chain left-side flow-control output
XOFFRo	O	chip-to-chip serial chain right-side flow-control output
L1DCLdOut [50:0]	I	output word from the L1-DCL
L1push	I	push (write-enable) signal from L1-DCL
R3DCLdOut [50:0]	I	output word from the R3-DCL
R3push	I	push (write-enable) signal from the R3-DCL
CSRdOut[31:0]	I	output value from Control/Status/Register system
CSRpush	I	push (write-enable) signal from Control/Status/Register system
L1DCLFifoFull	O	indicator that the readOut L1-DCL fifo is full
R3DCLFifoFull	O	indicator that the readOut R3-DCL fifo is full

Table 3-11 : Readout Logic Input/Output Signal Definitions

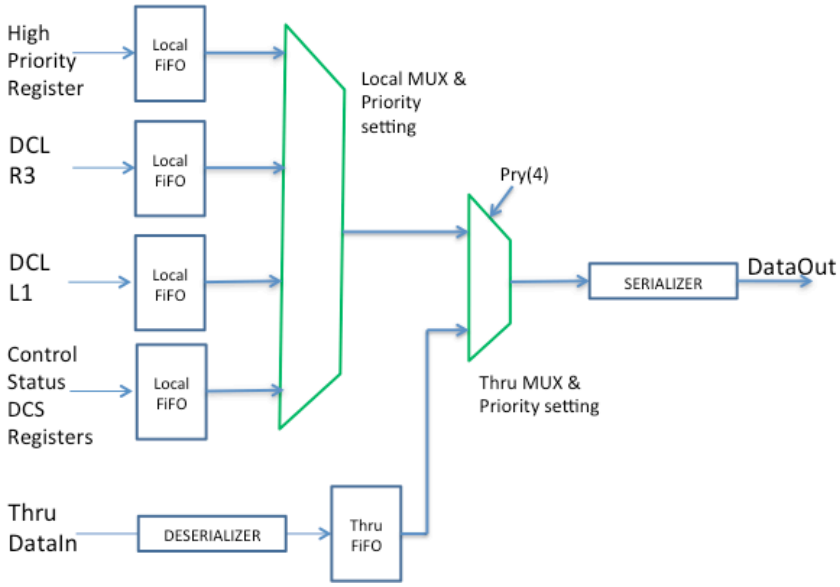


Figure 3-8 Readout logic blocks showing the 5 FIFO containing pending data packets

The readout circuitry is responsible for receiving data packets from the adjacent chip, from the 2 DCL blocks and from the registers to be read. A priority mechanism defines the order in which packets are formatted and then sent out serially. The priority order is shown in the table NN, for the 2 possible configurations of the data packets order.

There are 5 interface FIFOs. One is receiving the data from the adjacent chip (ThruFIFO), and four are receiving data from the current chip (LocalFIFO): 2 FIFO are attached to the 2 DCL outputs (physics data), one FIFO is receiving the Special Status Register with high priority, one FIFO is receiving the other internal registers data.

A first priority mechanism is fixed by a priority number attributed to a chip depending on its position in a readout chain. This priority number (Pry) fixes the number of packets from adjacent chips passing through the current chip versus the number of packets issued from the current chip. The priority number goes from 1 to 5 in a chain of 5 chips: the first ABC with priority one transmits only internal packets (this chip has no adjacent), the second ABC has a priority 2, and then transmits one packet over 2 with the sequence internal-adjacent (provided there is pending adjacent data), the next chip has priority 3, transmits with the order adjacent-adjacent-internal, etc …. The last chip in a chain of 5 would transmit with priority of 4 adjacent packets for one internal packet.

A second priority mechanism is predefined in every chip according to the following order:

- Adjacent packet (within the priority order as detailed above)
- High Priority Status Register data (if enabled)
- R3-DCL packet
- L1-DCL packet
- Register data (obtained by issuing Read Register commands)

The mechanism of transmitting packets can be described as this: if there is pending adjacent data, then the packet is transmitted, according to the fixed priority number for sequencing adjacent or internal data predefined by the chip position in the readout chain. If no adjacent packet or if the fixed priority number gives the hand to the internal data, the readout block checks the FIFOs not empty flags in the order High Priority Register (if enabled), R3_DCL packet, L1-DCL packet, Register data.

The FIFOs are sized (by simulation cases) in such a way that the probability of overfilling the FIFOs with physics data packets (Adjacent, R3_DCL, L1-DCL) should be kept low. An overfilling would result into a loss of the new data, until some location is available into the FIFO(*). It should be noted that the adjacent FIFO is protected from overfilling by the Xoff mechanism described in paragraph XX.

A special case is the FIFO with the Register Data: it has the lowest priority and gets its data from issuing read commands to the chip. In case of overfilling, the last commands will result in no available responses, and it will be the responsibility of the system control to detect and limit the read commands overfilling.

(*): the opposite may be built in : the latest incoming data are overwriting the old ones.

The readout part receives the adjacent chip data through a deserializer running at 160Mb/s. It receives 60 bits of data as soon as a "one" is sensed at the input. The signal Xoff is going to be one if the readout is not in a state to receive 60 more bits, should the data input be sensed to one. The Xoff is sent as an output to the adjacent chip to prevent it sending the 60 consecutive bits forming a packet.

Each packet selected by the readout priority mechanisms is transmitted to the fast 160Mb/s serializer. The header bit (one) is presented to the output, and if the Xoff state of the next chip is low, the 60 consecutive bits forming the packet are transmitted (and accepted by the next chip, as "adjacent chip" data packet). If the Xoff sate of the next chip is high, the serializer waits until it is going low before transmitting the packet.

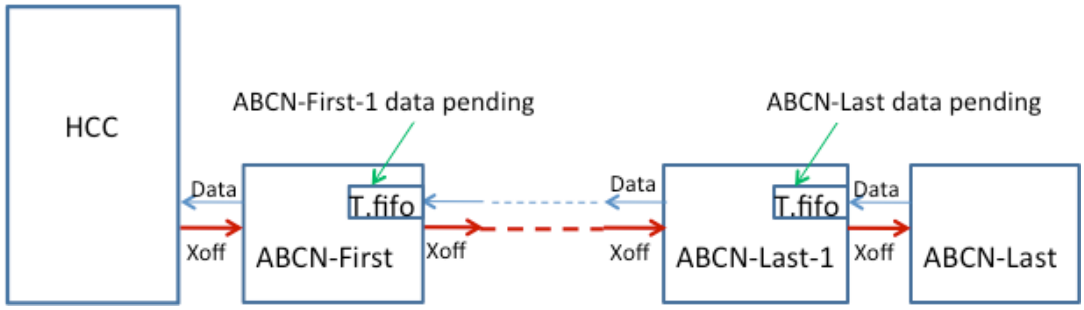


Figure 3-9: Data and Xoff signal direction in one example of reading several ABC chips with control by the HCC.

3.1.16 Readout Packet Format

In ABC 130 there is a unique readout packet format. It is made of a "Header" part containing event identification and data type, and of a "Payload" containing the cluster information of physics data requested by R3 or L1 Trigger inputs or other type of information requested by commands.

There are 2 types of physics data : cluster information coming from a R3 readout request, cluster information coming from a L1 readout request, with 2 possible modes.

There are non-physics data, with basically are made of register identification and registers contents (status, flags, SEU detection, configuration, input patterns, analogue bias setting …).

The packet contains 60 bits as shown below:

26 bits Header	34 bits Payload
60 bits packet size	

3.1.16.1 PHYSICS DATA HEADER:

Table 3-12 : Packet Header (Physics Data)

Start Bit	ChipID	TYP	L0ID	BCID
1	5	4	8	8

The Header is made of 26 bits arranged as shown in **Error! Reference source not found.**:

The ChipID Field contains the physical chip address of 5 bits, hardwired on the hybrid.

L0ID and BCID fields are the event identifiers.

The TYP field identifies the packet information :

Table 3-13 : TYP Descriptor in output packets

TYP code	Meaning
0000	Not used
0001	Reserved (super packet?)
0010	R3 packet (with hits)
0011	R3 packet (no hits)
0100	L1-1BC packet (with hits)
0101	Not used
0110	L1-1BC packet (last packet)
0111	L1-1BC packet (no hits)
1000	Read Register Packet
1001	Status Register Packet
1010	DCS Packet
1011	Undefined (will be)
1100	L1-3BC packet (with hits)
1101	Not used
1110	L1-3BC packet (last packet)
1111	L1-3BC packet (no hits)

3.1.16.2 NON PHYSICS DATA HEADER:

Table 3-14 : Packet Header (Non Physics Data)

Start Bit	ChipID	TYP	Address	TBD
1	5	4	8	N0000000

The Header is made of 26 bits arranged as shown in Table 3-14:

The Address bits field identifies the register (location) of the packet information. The 8 last bit of the Header are made of one bit of SEU check followed by 7 zeros.

3.1.16.3 PHYSICS DATA R3 PAYLOAD:

Table 3-15 : R3 packet (4 clusters)

Address	Address	Address	Address	OvF	Stop Bit
8	8	8	8	1	1

The PayLoad has 34 bits : 32 bits are made of 4 consecutive 8 bits “channel addresses”(*). Each channel address points to a cluster “center” identified with the R3DCL criteria. If no cluster was found, there is a specific packet TYP in the Header, and the PayLoad contains UNDEFINED data. If less than 4 clusters are found, the last cluster address is repeated in the available Address slots. If there are more than 4 clusters detected only one packet is sent, but the OverFlow bit (OvF) is set to one. The last bit of the PayLoad is a STOP bit at one.

3.1.16.4 PHYSICS DATA L1-1BC PAYLOAD

Table 3-16: L1-1BC packet (3 clusters)

Address	Hit	Address	Hit	Address	Hit	Stop Bit
8	3	8	3	8	3	1

The PayLoad has 34 bits : There are 3 consecutive “cluster data” of 11 bits each : a cluster data contains the 8 bits channel address(*) of the first hit in the cluster (in the scanning order defined by the L1DCL) followed by 3 bits showing hit or no-hit in the 3 next channels for the same row of strips. If no cluster was found, there is a specific packet TYP in the Header, and the PayLoad contains UNDEFINED data. If less than 3 clusters are found, the last cluster data is repeated in the available cluster data slots. If more than 3 clusters are found, a new packet (Header and PayLoad) is built along the same rules. A specific data TYPE identifies the last packet of an event. The last bit of the PayLoad is a STOP bit at one.

3.1.16.5 PHYSICS DATA L1-3BC PAYLOAD:

Table 3-17: L1-3BC packet

Address	Hit	Hit	Hit	Hit	TBD	End Bit
8	3	3	3	3	13	1

The PayLoad has 34 bits : There is 1 “extended cluster data” of 20 bits followed by 13 bits to be DEFINED : the extended cluster data contains the 8 bits channel address(*) of the first hit in the cluster (in the scanning order defined by the L1DCL) followed by the hit information on 3 bunch crossings for the first channel and for the 3 next channels in the same row of strips. The hit information per channel is made of the hit data at the bunch crossing before, the one current and the next one. If no cluster was found, there is a specific packet TYP in the Header, and the PayLoad contains UNDEFINED data. If more than 1 cluster is found, a new packet (Header and PayLoad) is built along the same rules. A specific data TYPE identifies the last packet of an event. The last bit of the PayLoad is a STOP bit at one.

(*) : in data packets the channels addresses are following the number order as defined in column 1 of Table 3-5

3.1.16.6 NON PHYSICS DATA PAYLOAD:

Table 3-18: L1-3BC packet

Data	TBD	End Bit
32	1	1

The PayLoad has 34 bits : There are 32 bits for the register data and one UNDEFINED bit. The last bit of the PayLoad is a STOP bit at one.

3.1.16.7 STOP bit

The “STOP” bit may be used as a primary indicator of the internal status of a chip. Its normal state would be one, but if zero it would indicate a special condition occurs. For example full FIFO flags could be reported to that indicator.

3.1.17 Beam Crossing Counter

This is an 8-bit binary counter which is incremented on every clock cycle. This counter is zeroed by either hardware reset, a software reset, or a special BC Reset Command. The BC counter value is entered in the pipeline at each clock cycle and transferred to the readout buffer at the time of a L1 signal receipt.

3.1.18 L0ID Counter

This a 8-bit binary counter which is incremented every time the chip receives a L0 trigger. The counter is set to $FF by either a hardware reset or software reset. The L0ID counter is used as the address for data transferred out of the pipeline. Both the R3 and L1 trigger use L0ID to index into the L0Buffer to get the data selected by the trigger system.

3.1.19 Command Decoder

In ABC 130 there are three classes of commands: “RESET” (8-bit command format), “ACSR” and “SPECIAL” (58-bit command format). Reset commands are global and have a direct effect on the chips operation: they are used to resynchronize the BC and Trigger counters, and eventually they return the chip in predefined default states (states to be DEFINED).

ACSR “Access Control and Status Registers” commands are global or addressable commands to execute Write or Read operations into the internal registers. The ACSR commands with Read should not interfere with the data taking operation, however there may be limitations if such commands are received when the chip is in data taking mode (limitations to be DEFINED).

SPECIAL commands have the same format as ACSR, they use the specific register address $00, but the commands are interpreted to perform a specific operation in the chip like: send a calibration pulse, a digital test pulse, activate test modes, or control the write access to the registers (to prevent a chip to be accidentally reconfigured during physics data taking).

Table 3-19 : Short and Long Commands

Type	Header	Field 2 (Type)	Field 2 Parity	Next Fields	Description
Default	1010	000	0	NO	FastClusterFinder Reset
Reset	1010	001	1	NO	SYS Reset
Reset	1010	010	1	NO	BC Reset
Reset	1010	011	0	NO	L0ID Preset *
Reset	1010	100	1	NO	Soft Reset
Reset	1010	101	0	NO	SEU registers Reset
HCC	1011	110	1	50 bits	HCC commands
ABC	1011	111	0	50 bits	ABC commands

- : The default Preset at Power-Up is $FF. The L0ID Preset value can be modified by writing 1 in the bit 16 of the configuration register $22 and setting the preset value in bits 8 to 15 of the same register.

3.2 RESET Commands:

In the case of the ABC 130 chip, different reset commands have been defined, i.e. the Soft Reset, BC Reset commands, L0ID counter Preset command, SEU registers reset. It is expected that these commands will be sent to the chip at regular intervals during periods of time when no triggers signals will be sent to the chip. The purpose of these commands is to perform controlled resets of the chip. (see section 3.2.19 for details).

The “Idle” command is not interpreted. However it is received and decoded to avoid being interpreted as a wrong command.

3.3 ACSR commands

These are long packets that enable the operation of the chip to be controlled by setting bits in registers. Only the addressed chips will act on the packet, unless the address sent equals '1111', in which case all chips will act on the packet. All chips that receive the packet must decode it, even if they do not act on it. This is to avoid un-addressed chips erroneously decoding parts of the data field as the start of packets. Write and Read ACSR commands can be sent to the chip during normal data taking (ie. at the same time as L0, R3 or L1 inputs). Read commands are taking the lowest priority: the register content addressed by the Read command will be sent out only if R3 or L1 packet buffers are empty. Write commands executions can be switched-off by setting a bit in the Special Command, to prevent a chip to be accidentally reconfigured.

Table 3-20 : WACSR Commands (Write)

Field 3 5 bits HCC ChipID	Field 4 5 bits ABC ChipID	Field 5 7 bits Register address	Field 6 1 bit (R/W)	Field 7 (32 bits) Data	Description
aaaaa	aaaaa	$00	1/Write Only	32hddddddddd	Special Register
aaaaa	aaaaa	$0F-$01	1	32hddddddddd	ANALOG and DCS
aaaaa	aaaaa	$17-$10	1	32hddddddddd	MASK Input Registers
aaaaa	aaaaa	$1F-$18	1	32hddddddddd	PATTERN Input Registers
aaaaa	aaaaa	$2F-$20	1	32hddddddddd	CONFIG Registers
aaaaa	aaaaa	$3E-$30	(Read-Only)	32hddddddddd	STATUS and SEU Registers
aaaaa	aaaaa	$3F	(Read-Only)	32hddddddddd	High Priority Register
aaaaa	aaaaa	$5F-$40	1	32hddddddddd	LSB TrimDAC Registers
aaaaa	aaaaa	$67-$60	1	32hddddddddd	MSB TrimDAC Registers
aaaaa	aaaaa	$6F-$68	1	32hddddddddd	Calibration Registers

N.B.

xxx = don't care state.

aaaa = 5 bits chip address(MSB bit first)

8hddddddddd = 32 bits values for registers (MSB bit first)

Field 3

This is the 5 bit reserved for the HCC ChipID. '11111' is used as the broadcast address. This field is not interpreted by ABC130 chips.

Field 4

This is the 5 bit of the ABC130 ChipID. '11111' is used as the broadcast address.

Field 5

The register addresses are distributed in ranges of 16 consecutive addresses per part of the chip. There can be unused bits per register and unused addresses in the range. Precise definition of the register content per address will be part of each block functional description.

Field 6

This bit is one if command is to Write in register, 0 if command is to Read register.

Field 7

This field holds the 32 bits data that is to be written into the selected register.

Registers banks are separated in groups :

ANALOG and DCS : Write and Read registers, default setting at reset, TBD. Write protected by a bit set in Register $00.

INPUT : Mask bits (also test pattern injection), Write and Read, masked by default at reset ? (to avoid noisy signals propagation at startup?). Write protected by a bit set in Register $00.

CONFIGURATION : Configuration bits, Write and Read, Preset value at reset. Write protected by a bit set in Register $00.

STATUS and SEU : Read only registers. The STATUS register at address $37 is defined as the high priority Status Register. SEU registers are reset by the OR of SoftResetb and the specific SEU Reset command.

TrimDAC and Calibration : Write and Read registers, default setting at reset. Write protected by a bit set in Register $00.

Table 3-21 : RACSR Commands (Read)

Field 3 5 bits HCC ChipID	Field 4 5 bits ABC ChipID	Field 5 7 bits Register address	Field 6 1 bit (R/W)	Field 7 (32 bits) Data	Description
aaaaa	aaaaa	$00	(Write Only)	32hddddddddd	Special Register
aaaaa	aaaaa	$0F-$01	0	32hddddddddd	ANALOG and DCS
aaaaa	aaaaa	$17-$10	0	32hddddddddd	MASK Input Registers
aaaaa	aaaaa	$1F-$18	0	32hddddddddd	PATTERN Input Registers
aaaaa	aaaaa	$2F-$20	0	32hddddddddd	CONFIG Registers
aaaaa	aaaaa	$3E-$30	0/Read Only	32hddddddddd	STATUS and SEU Registers
aaaaa	aaaaa	$3F	0/Read Only	32hddddddddd	High Priority Register
aaaaa	aaaaa	$5F-$40	0	32hddddddddd	TrimDACS <3.0> Registers
aaaaa	aaaaa	$67-$60	0	32hddddddddd	TrimDACs <4> Channels Registers
aaaaa	aaaaa	$6F-$68	0	32hddddddddd	CalEnable Registers

3.4 SPECIAL Commands:

This is a regular 58 bits long command, with the "register address" field set at '0000000': setting '1' in the 32 consecutive bits of the Data field, will generate an immediate specific command execution. Only the addressed chips will act on the command, unless the ABC130 address sent equals '1111', in which case all chips will act on the command. All chips that receive the command must decode it, even if they do not act on it. This is to avoid un-addressed chips erroneously decoding parts of the data field as the start of packets. The Special commands can be sent to the chip during normal data taking (ie. at the same time as L0, R3 or L1 inputs).

Table 3-22 : Special Commands (Interpreted field 7)

Field 3 5 bits HCC ChipID	Field 4 5 bits ABC ChipID	Field 5 7 bits Register address	Field 6 1 bit (R/W)	Field 7 (32 bits) Data	Description
aaaaa	aaaaa	$00	1	32hddddddddd	Special commands

The listed specific commands are (TB updated) :

Send Calibration Pulse

Send Digital Test Pulse

High Priority Register Clearing

Disables Write operation on physical registers (a control bit that can be read through one of the status registers). This bit is reset by the softReset signal or by any write to one to the bits in range 0 to 3.

Test cycle 1 (TBD)

Test cycle 2 (TBD)

3.4.1.1 SEU Protection

The logic for decoding the RESET commands and the "MODE" command acting on the WRITE registers enable/disable should be triplicated

REG type	TRIPLICATION	
ANALOG & DCS	YES	
MASK	YES	
CONFIG	YES	
STATUS & SEU	NO	
CHANNELS	YES	

Table 3-23: registers subject to triplication

The signals issued by the command decoder to operate write or read access to the protected registers do not need triplication: the probability to get false write is low (needs simultaneous corruption of two different signals). False read has no impact.

3.4.2 Registers

Table 3-24: SPECIAL REGISTER

Addresses : $00 (1 register of 32 bits)

	SCREg
	$00
31	0
30	0
29	0
28	0
27	0
26	0
25	0
24	0
23	0
22	0
21	0
20	0
19	0
18	0
17	0
16	0
15	0
14	0
13	0
12	0
11	0
10	0
9	0
8	0
7	0
6	0
5	0
4	WriteDisable
3	0
2	HPRClear
1	DigitalPulse
0	CalPulse
SEUbit	serSC
model	SCREg
Reset Value	00000000

Bit Functions :

CalPulse : Generate a calibration pulse, 200ns wide (8BC). The polarity is controlled by the bit 12 in register $21.

DigitalPulse : Generate a 1BC pulse at the input of the pipeline (Present version : not implemented)

HPRClear : High Priority Register flag bits clearing

Write disable : if set this bit prevents write commands on registers other than $00 to be active (protection against spurious commands). Any subsequent write command addressed to register $00 with one of the bits 0 to 3 at one clears the register and this bit.

Table 3-25: ANALOG AND DCS REGISTERS

Addresses : $01 to $0F (15 registers of 32 bits)

	ADCS1	ADCS2	ADCS3	ADCS4	ADCS5	ADCS6	ADCS7
	$01	$02	$03	$04	$05	$06	$07
31	0	0	0				A_EN_CTRL
30	0	0	0				A_S15
29	0	0	0				A_S14
28	BTRANGE(4)	BIPRE(4)	0				A_S13
27	BTRANGE(3)	BIPRE(3)	0				A_S12
26	BTRANGE(2)	BIPRE(2)	0				A_S11
25	BTRANGE(1)	BIPRE(1)	0				A_S10
24	BTRANGE(0)	BIPRE(0)	0				A_S9
23	0	0	BCAL(7)				A_S8
22	0	0	BCAL(6)				A_S7
21	0	0	BCAL(5)				A_S7
20	B8BREF(4)	BIFEED(4)	BCAL(4)				A_S6
19	B8BREF(3)	BIFEED(3)	BCAL(3)				A_S5
18	B8BREF(2)	BIFEED(2)	BCAL(2)				A_S4
17	B8BREF(1)	BIFEED(1)	BCAL(1)				A_S3
16	B8BREF(0)	BIFEED(0)	BCAL(0)			D_EN_CTRL	A_S2
15	0	0	0			D_S16	A_S1
14	0	0	0			D_S15	BTMUXD
13	0	0	STR_DEL(5)			D_S14	BTMUX(13)
12	BIREF(4)	COMBIAS(4)	STR_DEL(4)			D_S13	BTMUX(12)
11	BIREF(3)	COMBIAS(3)	STR_DEL(3)			D_S12	BTMUX(11)
10	BIREF(2)	COMBIAS(2)	STR_DEL(2)			D_S11	BTMUX(10)
9	BIREF(1)	COMBIAS1)	STR_DEL(1)			D_S10	BTMUX(9)
8	BIREF(0)	COMBIAS(0)	STR_DEL(0)			D_S9	BTMUX(8)
7	0	BVT(7)				D_S8	BTMUX(7)
6	0	BVT(6)				D_S7	BTMUX(6)
5	0	BVT(5)				D_S6	BTMUX(5)
4	BVREF(4)	BVT(4)				D_S5	BTMUX(4)
3	BVREF(3)	BVT(3)				D_S4	BTMUX(3)
2	BVREF(2)	BVT(2)				D_S3	BTMUX(2)
1	BVREF(1)	BVT(1)	STR_DEL_R(1)			D_S2	BTMUX(1)
0	BVREF(0)	BVT(0)	STR_DEL_R(0)			D_S1	BTMUX(0)
SEUbit	ADCS1SEU (serNC1)	ADCS2SEU (serNC2)	ADCS3SEU (serNC3)			ADCS6SEU (serNC6)	ADCS7SEU (serNC7)
model	reg32tr	reg32tr	reg32tr			reg32tr	reg32tr
Reset Value	00000000	000000FF	00000000			00000000	00000000

Bit Functions :

See the Front-end section for the bias under control by each bits group. The default sets all bias currents to the minimum, the discriminator voltage (BVT) to the maximum, the calibration pulse delay and amplitude to zero or minimum, the MUX output is not enabled, and the regulators output value tuning are non active. The regulator outputs are set to the maximum.

A_EN_CTRL : at one activates the output voltage tuning with bits A_S1 to A_S7. At zero the regulator output is at maximum voltage.

D_EN_CTRL : at one activates the output voltage tuning with bits D_S1 to D_S7. At zero the regulator output is at maximum voltage.

Table 3-26: INPUT (MASK) REGISTERS

Addresses : $10 to $17 (8 registers of 32 bits)

	MaskInput0	MaksInput1	MaksInput2	MaksInput3	MaksInput4	MaskInput5	MaskInput6	MaskInput7
	$10	$11	$12	$13	$14	$15	$16	$17
31	ch31	ch63	ch95	ch127	ch159	ch191	ch223	ch255
30								
29								
28								
27								
26								
25								
24								
23								
22								
21								
20								
19								
18								
17								
16								
15								
14								
13								
12								
11								
10								
9								
8								
7								
6								
5								
4								
3								
2								
1								
0	ch0	ch32	ch64	ch96	ch128	ch160	ch192	ch223
SEUbit	MT0SEU	MT1SEU	MT2SEU	MT3SEU	MT4SEU	MT5SEU	MT6SEU	MT7SEU
model	reg32tr	reg32tr	reg32tr	reg32tr	reg32tr	reg32tr	reg32tr	reg32tr
Reset state	00000000	00000000	00000000	00000000	00000000	00000000	00000000	00000000

The Input (Mask) Registers bits are used to

1) Mask the channel when bit TM is clear (bit 16 of register $20). Channels are numbered from 0 to 255 in the same order as the front-end channels (column 2 in Table 3-5).
2) Inject a fixed pattern in the L0 pipeline if bit TM is set (bit 16 of register $20)

Table 3-27: INPUT Pattern REGISTERS

Addresses : $18 to $1F (8 registers of 32 bits)

	RegInput0	RegInput1	RegInput2	RegInput3	RegInput4	RegInput5	RegInput6	RegInput7
	$18	$19	$1A	$1B	$1C	$1D	$1E	$1F
31	ch31	ch63	ch95	ch127	ch159	ch191	ch223	ch255
30								
29								
28								
27								
26								
25								
24								
23								
22								
21								
20								
19								
18								
17								
16								
15								
14								
13								
12								
11								
10								
9								
8								
7								
6								
5								
4								
3								
2								
1								
0	ch0	ch32	ch64	ch96	ch128	ch160	ch192	ch223
SEUbit	no	no	no	no	no	no	no	no
model	reg32ro	reg32ro	reg32ro	reg32ro	reg32ro	reg32ro	reg32ro	reg32ro
Reset state	00000000	00000000	00000000	00000000	00000000	00000000	00000000	00000000

The Input Pattern Registers bits are read-only registers loaded at each bunch crossing with the hit pattern at the L0 pipeline input.

The channel numbering is the one described in paragraph “Channel Numbering”: numbered from 0 to 255 with the same order as the front-end inputs (column 2 in Table 3-5).

Table 3-28: CONFIGURATION REGISTER

Address Range $20 to $2F is reserved for configuration registers (16 registers of 32 bits). Actually 4 registers are defined from $20 to $23.

	$20	$21	$22	$23
31	0	0	0	0
30	0	0	0	0
29	FCcontrol(1).	0	0	0
28	FCcontrol(0).	0	0	0
27	0	0	0	0
26	0	0	0	0
25	0	0	0	0
24	0	0	0	SEUCNT_E
23	0	0	0	0
22	0	0	0	0
21	0	0	0	0
20	0	0	0	two_cluster
19	0	0	0	0
18	0	0	0	Limit_Enable
17	TM(1)	0	0	Packet_Limit(5)
16	TM(0)	0	L0IDPreset.	Packet_Limit(4)
15	0	0	PreL0ID(7).	Packet_Limit(3)
14	0	0	PreL0ID(6).	Packet_Limit(2)
13	0	0	PreL0ID(5).	Packet_Limit(1)
12	ThruEnable	CalPulsePolarity	PreL0ID(4).	Packet_Limit(0)
11	CRSa enable.	0	PreL0ID(3).	0
10	L1 enable.	FCDriv(2).	PreL0ID(2).	0
9	R3 enable.	FCDriv(1).	PreL0ID(1).	TopR(5).
8	CSRb enable.	FCDriv(0).	PreL0ID(0).	TopR(4).
7	0	0	Latency(7).	TopR(3).
6	0	CurrDrivR(2).	Latency(6).	TopR(2).
5	L0mode	CurrDrivR(1).	Latency(5).	TopR(1).
4	Dir.	CurrDrivR(0).	Latency(4).	TopR(0).
3	pry(3).	0	Latency(3).	EN_01.
2	pry(2).	CurrDrivL(2).	Latency(2).	mcluster.
1	pry(1).	CurrDrivL(1).	Latency(1).	L1DCL mode(1).
0	pry(0).	CurrDrivL(0).	Latency(0).	L1DCL mode(0).
SEUbit	CFG0SEU(serI)	CFG1SEU(serJ)	CFG2SEU(serK)	SFG3SEU(serL)
model	reg32tr	reg32tr	reg32tr	reg32tr
Reset Value	00000000	00000444	0000000F	00000000

Bit Functions :

Register $20 :

Pry(3:0) sets the priority number for the thru packets in the chip

Dir sets the DATA transmission direction. Dir at zero pushes data from “DATAL” (input) to “DATAR” (output), Dir at one pushes data from “DATAR” (input) to “DATAL” (output)

Dir sets the XOFF signal direction. Dir at zero sets XOFFL as an output and XOFFR as an input. Dir at one sets XOFFL as an input and XOFFR as an output.

L0mode controls the L0 signal interpretation: if L0mode is zero, a single pulse at 40Mb/s is interpreted as one L0 signal. If L0mode is one, the pattern 110 at 40Mb/s is interpreted as one L0 signal.

CSRb_enable, R3_enable, L1_enable, CSRa_enable, ThruEnable are bits to enable (1) or disable (0) the transmission of data originating from : the SCRb FIFO containing read registers command outputs, the R3 (resp. L1) FIFO containing R3 or L1 physics packets, the CSRa FIFO containing the High Priority Register data, the Thru FIFO containing the data from adjacent chip. Disabling a FIFO does not prevent it to fill up, and may result in the FIFO full/overflow flags going high.

TM(0) : this bit needs to be set to one to swap the input (Mask) Registers contents to a fixed pattern inputs to the L0 pipeline.

FCcontrol(1:0) : 2 bits to control the operation of the FastClusterFinder (see the FasClusterFinder paragraph).

Register $21 :

CurrDriveL(3:0) : set current drive of DATAL and XOFFL outputs

CurrDriveR(3:0) : set current drive of DATAR and XOFFR outputs

CurrDriveFC(3:0) : set current drive of the FastClusterFinder outputs

CalPulsePolarity swaps the 8BC wide calibration pulse polarity

Register $22 :

Latency(7:0) sets the latency in the L0 pipeline in number of BC clocks (default at reset is 16)

PreL0ID(7:0) is the preset value of the internal L0ID counter (default is $00)

L0IDPreset : with this bit at zero the L0ID number starts from $FF (hence has the zero value at reception of the first L0 after a SoftReset or L0IDReset command). With this bit at one the start value is given by the PreL0ID byte.

Register $23 :

DCL(1:0) are bits controlling the L1DCL compression criteria according to Table 3-7

Mcluster : at zero sets the physics packet format in “3BC” mode, at one the physics packet format is “1BC”

EN_01 : enables the cluster finding by zero to one detection in the R3DCL.

TopR(5:0) : After the decoding of a L1L0ID command, the corresponding hits are transferred from the L1BUFFER to the L1DCL, with a delay fixed by the topR in number of BC clocks. This feature can be used to have the DCL activity occurring at different time after a L1L0ID is received by a group of ABC-130 chips.

Packet_Limit(5:0) : if the bit Limit_Enable is set, this bits value fixes the maximum number of packets send after a L1 Trigger.

Limit_Enable : at one limits the number of packets to the value represented in Packet_Limit bits. At zero the number of packets is limited to the maximum possible number of packets per L1 trigger ie. 64 in 3BC mode and 22 in 1BC mode.

Table 3-29: STATUS REGISTER $30 (-$3E)

Addresses range $30 to $3E is reserved for Status Registers (15 registers of 32 bits)

	STAT0	STAT1	STAT2
	$30	$31	$32
31	0		
30	CR47SEU		
29	CR43SEU		
28	CR39SEU		
27	CR35SEU		
26	CR31SEU		
25	CR27SEU		
24	CR23SEU		
23	CR19SEU		
22	CR15SEU		
21	CR11SEU		
20	CR7SEU		
19	CR3SEU		
18	MT7SEU		
17	MT6SEU		
16	MT5SEU		
15	MT4SEU		
14	MT3SEU		
13	MT2SEU		
12	MT1SEU		
11	MT0SEU		
10	TopLSEU		
9	SCRegSEU	aCSR OVFL	
8	ADCS7SEU	Thru OVFL	
7	ADCS6SEU	L1 OVFL	LocalL0ID(7)
6	ADCS3SEU	R3 OVFL	LocalL0ID(6)
5	ADCS2SEU	bCSR OVFL	LocalL0ID(5)
4	ADCS1SEU	aCSR Full	LocalL0ID(4)
3	CFG3SEU	Thru Full	LocalL0ID(3)
2	CFG2SEU	L1 Full	LocalL0ID(2)
1	CFG1SEU	R3 Full	LocalL0ID(1)
0	CFG0SEU	bCSR Full	LocalL0ID(0)
SEUbit	no	no	no
model	reg32ro	reg32ro	reg32ro
Reset Value	00000000	00000000	00000000

Register $30 :

This register contains the SEU flags generated in the triplicated various registers (if one SEU occurs, the protected register value may not change because of the triplication but the SEU bit flag is set)

Register $31 :

This register contains the Overflow and Full flags of the 5 FIFOs containing data to transmit (ThruFIFO, aCSR, L1, R3, bCSR). “Full” indicates that the next write in the FIFO will overwrite data but data has currently not been overwritten. “Overflow” indicates that one overwrite at least as occurred, hence the oldest data is lost.

Register $33 :

FastClusterFinder cluster counters values (not implemented)

Register $34 :

eFuse Register Data (Unique Chip Identification)(not implemented)

Table 3-30: HIGH PRIORITY REGISTER $3F

Address $3F is reserved for the aCSR High Priority Register (register of 32 bits)

	STATF(aCSR)
	$3F
31	
30	
29	
28	
27	
26	
25	
24	
23	
22	
21	
20	
19	
18	
17	
16	
15	
14	
13	
12	
11	
10	
9	aCSR OVFL
8	Thru OVFL
7	L1 OVFL
6	R3 OVFL
5	bCSR OVFL
4	aCSR Full
3	Thru Full
2	L1 Full
1	R3 Full
0	bCSR Full
SEUbit	no
model	reg32ro
Reset Value	Readonly

This register actually contains the full and overflow flags of the 5 readout FIFOs.

Table 3-31: TRIMDAC REGISTERS ($40 to $67, 40 registers)

Each 32 bits register in the range $40 to $5F contains the 4 LSB bits of the TrimDAC for 8 channels. In such a way an 8-bit byte contains the value for 2 channels.

Each 32 bits register in the range $60 to $6F contains the MSB bit of the TrimDAC for 32 channels.

The channel numbering is the one described in paragraph “Channel Numbering”: numbered from 0 to 255 with the same order as the front-end inputs (column 2 in Table 3-5).

	TrimDAC0-31	TrimDAC32-40
	$40 to $5F	$60 to $67
31	TRIMDAC<3> CH7:mod8	TRIMDAC<4> CH31:mod32
30	TRIMDAC<2> CH7:mod8	TRIMDAC<4> CH30:mod32
29	TRIMDAC<1> CH7:mod8	TRIMDAC<4> CH29:mod32
28	TRIMDAC<0> CH7:mod8	TRIMDAC<4> CH28:mod32
27	TRIMDAC<3> CH6:mod8	TRIMDAC<4> CH27:mod32
26	TRIMDAC<2> CH6:mod8	TRIMDAC<4> CH26:mod32
25	TRIMDAC<1> CH6:mod8	TRIMDAC<4> CH25:mod32
24	TRIMDAC<0> CH6:mod8	TRIMDAC<4> CH24:mod32
23	TRIMDAC<3> CH5:mod8	TRIMDAC<4> CH23:mod32
22	TRIMDAC<2> CH5:mod8	TRIMDAC<4> CH22:mod32
21	TRIMDAC<1> CH5:mod8	TRIMDAC<4> CH21:mod32
20	TRIMDAC<0> CH5:mod8	TRIMDAC<4> CH20:mod32
19	TRIMDAC<3> CH4:mod8	TRIMDAC<4> CH19:mod32
18	TRIMDAC<2> CH4:mod8	TRIMDAC<4> CH18:mod32
17	TRIMDAC<1> CH4:mod8	TRIMDAC<4> CH17:mod32
16	TRIMDAC<0> CH4:mod8	TRIMDAC<4> CH16:mod32
15	TRIMDAC<3> CH3:mod8	TRIMDAC<4> CH15:mod32
14	TRIMDAC<2> CH3:mod8	TRIMDAC<4> CH14:mod32
13	TRIMDAC<1> CH3:mod8	TRIMDAC<4> CH13:mod32
12	TRIMDAC<0> CH3:mod8	TRIMDAC<4> CH12:mod32
11	TRIMDAC<3> CH2:mod8	TRIMDAC<4> CH11:mod32
10	TRIMDAC<2> CH2:mod8	TRIMDAC<4> CH10:mod32
9	TRIMDAC<1> CH2:mod8	TRIMDAC<4> CH9:mod32
8	TRIMDAC<0> CH2:mod8	TRIMDAC<4> CH8:mod32
7	TRIMDAC<3> CH1:mod8	TRIMDAC<4> CH7:mod32
6	TRIMDAC<2> CH1:mod8	TRIMDAC<4> CH6:mod32
5	TRIMDAC<1> CH1:mod8	TRIMDAC<4> CH5:mod32
4	TRIMDAC<0> CH1:mod8	TRIMDAC<4> CH4:mod32
3	TRIMDAC<3> CH0:mod8	TRIMDAC<4> CH3:mod32
2	TRIMDAC<2> CH0:mod8	TRIMDAC<4> CH2:mod32
1	TRIMDAC<1> CH0:mod8	TRIMDAC<4> CH1:mod32
0	TRIMDAC<0> CH0:mod8	TRIMDAC<4> CH0:mod32
SEUbit	CR3SEU-CR31SEU	CR35SEU-39SEU
model	reg32tr	reg32tr
Reset state	00000000	00000000

Note : one SEU flag bit is generated for a group of 4 registers. For the 40 TrimDAC registers there are 10 SEU bit names : CR3SEU CR7SEU CR11SEU CR15SEU CR19SEU CR23SEU CR27SEU CR31SEU CR35SEU CR39SEU.

Table 3-32: Calibration Enable REGISTERS ($68 to $6F, 8 registers)

Each 32 bits register contains 1 bit per channel enabling the calibration pulse.

The channel numbering is the one described in paragraph “Channel Numbering”: numbered from 0 to 255 with the same order as the front-end inputs (column 2 in Table 3-5).

	CalREG0-7
	$68 to $6F
31	CAL_EN CH31:mod32
30	CAL_EN CH30:mod32
29	CAL_EN CH29:mod32
28	CAL_EN CH28:mod32
27	CAL_EN CH27:mod32
26	CAL_EN CH26:mod32
25	CAL_EN CH25:mod32
24	CAL_EN CH24:mod32
23	CAL_EN CH23:mod32
22	CAL_EN CH22:mod32
21	CAL_EN CH21:mod32
20	CAL_EN CH20:mod32
19	CAL_EN CH19:mod32
18	CAL_EN CH18:mod32
17	CAL_EN CH17:mod32
16	CAL_EN CH16:mod32
15	CAL_EN CH15:mod32
14	CAL_EN CH14:mod32
13	CAL_EN CH13:mod32
12	CAL_EN CH12:mod32
11	CAL_EN CH11:mod32
10	CAL_EN CH10:mod32
9	CAL_EN CH9:mod32
8	CAL_EN CH8:mod32
7	CAL_EN CH7:mod32
6	CAL_EN CH6:mod32
5	CAL_EN CH5:mod32
4	CAL_EN CH4:mod32
3	CAL_EN CH3:mod32
2	CAL_EN CH2:mod32
1	CAL_EN CH1:mod32
0	CAL_EN CH0:mod32
SEUbit	CR43SEU-CR47SEU
model	reg32tr
Reset state	00000000

Note : one SEU flag bit is generated for a group of 4 registers. For the 8 TrimDAC registers there are 2 SEU bit names : CR43SEU CR47SEU.

3.4.3 Chip ID

The ABC 130 chip address field is 5 bits, different from the ABCD case, where it was 6 bits (and only 4 bits transmitted).

To enable a chip to be individually addressed four inputs ID(4:0) will be used to implement a geographical addressing scheme. This is because there may be more than 16 chips to be addressed on each hybrid. These inputs will be wire bonded to a unique set of logic levels for each chip. This set of logic levels will form a geographical address that will enable individual chips on the hybrid to be addressed. Each address input has an internal pull-up. The address "11111" (15) is reserved for global addressing (all chips respond).

3.4.4 Chip Initialisation and Configuration

3.4.5 Resets

There are three kinds of reset in the system.

3.4.5.1 Power up reset

The power-up reset is an asynchronous (i.e. clock independent) reset that sets the value of the chips registers to their default value, and clears all the buffers in the chip, thus placing the chip into a well defined state. This type of reset is issued automatically when power is first applied to the chip. Provision will be made to enable this signal to be supplied externally to the chip, through the input RSTB_pad.

3.4.5.2 Reset by Long R3-L1 input state

An alternative method for resetting the circuit is to provide more than 32 consecutive BC wide "one" state on the R3-L1 input. The reset action is similar to the one provided by the power up reset or external Reset through RSTB_pad. It requires that the BC clock is present.

3.4.5.3 Soft Reset

This type of reset is sent to the chip via a command instruction. Its purpose is to reset all the registers to their default value, and clears the pointers and readout mechanism, hence loosing the chip configuration and the physics data. It should result in a chip being in the same status as after a power-up reset.

3.4.5.4 BC Reset

This type of reset is sent to the chip via a command instruction. Its purpose is to zero the Beam Crossing counter. It has no effect on the operation of any other part of the chip.

The following sequence of instructions should normally be sent to the chip after power-up

1) Send command to load the configuration register with the appropriate settings.

2) Send a command to load the mask register

3) Send a series of commands to load the DAC register/s and Delay registers

The chip will now be in a state to receive L0 and R3 or L1 trigger commands and send data.

3.4.5.5 L0ID Reset

This type of reset is sent to the chip via a command instruction. Its purpose is to preset the Beam Crossing counter. It has no effect on the operation of any other part of the chip. If the bit 16 in the configuration register $22 is at zero the L0ID preset value is $FF (hence first L0 is identified with number $00). If the bit 16 in the configuration register $22 is at one the L0ID preset value is given by the bits 8 to 15 in the configuration register $22.

3.4.5.6SEU Reset

This type of reset is sent to the chip via a command instruction. Its purpose is to reset the bits tagging SEU events in the register $30.

3.4.5.7SYS Reset

This type of reset is sent to the chip via a command instruction. Its purpose is to clear all the buffers in the chip, while leaving the configuration of the chip unaffected. This type of reset will be issued to the chip periodically during data taking to eliminate synchronisation errors.

1) Upon receipt of the SYSReset command, the ABC-130 chip resets all internal counters and clears pending operations. If it was transmitting data, it terminates this immediately.

2) The external system must wait a time consistent with any data in the serial chain at the reset clock cycle to flush through the chain.

N.B. It should be noted that the off-detector system must then be able to determine the last complete event transmitted before the reset and discard it (Complete in the sense that all read-out chains supply a complete event). With either reset it must also be able to recognise and discard partial events since there is no guarantee that different read-out chains will be reading the same event when the periodic reset arrives.

3.4.6 Default Register Values

On power up or SoftReset command, the contents of the configuration registers will be set to default. This results in the following configuration (summary) :

Minimum Bias currents for the analogue channels

Maximum channel threshold value

TrimDACS setting at 0

All calibration enable at 0

SLVS drivers current at mid-range

L0 counter at $FF and BC counter at $00

Readout Priority value at $00

Data direction from left to right

Readout FIFO are disabled

Input register in Mask mode

L0 buffer latency at $0F

L0ID preset at $00, preset function disabled

L1DCL detection mode 00

L1DCL-3BC packet enabled

R3 DCL edge detection disabled

L1Buffer to L1DCL delay function at $00

No packet number limit

3.4.7 Input/Output Connections

The pin list is provided for the ABC130 design on the following Table 3-33.

	rate (MHz)	direction	Type	
module ABCN13 (				
//bottom edge signals				
BC_padN	160	I	SLVS	40MHz clock input
BC_padP	160	I	SLVS	40MHz clock input
CLK_padN	40	I	SLVS	Readout rate clock input
CLK_PadP	40	I	SLVS	Readout rate clock input
COM_LZERO_padN	80	I	SLVS	Multiplexed COM L0 input (80Mb/s)
COM_LZERO_padP	80	I	SLVS	Multiplexed COM L0 input (80Mb/s)
LONERTHREE_padN	80	I	SLVS	Multiplexed R3 L1 input (80Mb/s)
LONERTHREE_padP	80	I	SLVS	Multiplexed R3 L1 input (80Mb/s)
padDisable_RegA	Static	I	CMOS Pull-Down	Disable Regulator (Analogue)
padDisable_RegD	Static	I	CMOS Pull-Down	Disable Regulator (Digital)
padShuntCtrl	Analogue	I	Analogue	Shunt Device Control (analogue signal)
//data from the detector				
AIN[255:0]	40	I	Analogue	Inputs to FE channels
//right edge signals				
XOFFLB	160	I/O	SLVS	XOFF signal (bidirectional)
XOFFL	160	I/O	SLVS	XOFF signal (bidirectional)
DATLB	160	I/O	SLVS	DATA signal (bidirectional)
DATL	160	I/O	SLVS	DATA signal (bidirectional)
FastCLK_padN	320/640	I	SLVS	FastClusterFinder clock input
FastCLK_padP	320/640	I	SLVS	FastClusterFinder clock input
padTerm	Static	I	CMOS Pull-Down	SLVS Termination On/Off
padID(0:4)	Static	I	CMOS Pull-up	Chip Address (5 pads)
dataOutFC1_padN	320/640	O	SLVS	FastClusterFinder data output
dataOutFC1_padP	320/640	O	SLVS	FastClusterFinder data output
dataOutFC2_padN	320/640	O	SLVS	FastClusterFinder data output
dataOutFC2_padP	320/640	O	SLVS	FastClusterFinder data output
DATR	160	I/O	SLVS	DATA signal (bidirectional)
DATRB	160	I/O	SLVS	DATA signal (bidirectional)
XOFFR	160	I/O	SLVS	XOFF signal (bidirectional)
XOFFRB	160	I/O	SLVS	XOFF signal (bidirectional)
//top edge signals				
RSTB_pad	40	I	CMOS Pull-up	External Hard Reset signal
abcup_pad		I	CMOS Pull-Down	Reserved
SDO_BC	MHz	I	CMOS 8mA	Output for CLK Scan Path chain
SDI_BC	MHz	O	CMOS Pull-Down	Input for BC Scan Path chain
SDO_CLK	MHz	I	CMOS 8mA	Output for CLK Scan Path chain
SDI_CLK	MHz	O	CMOS Pull-Down	Input for BC Scan Path chain
Scan_Enable	Static	I	CMOS Pull-Down	Enable Scan Path chains
padTESTCOM	Analogue	O	Analogue	Discriminator bias "spy" point
TESTRES	Analogue	I	Analogue	Reference resistance
AMUXOUT	Analogue	O	Analogue	Analogue "spy" output
//Power pads				
4x GNDIT		Power	Analogue Ground	0V Analogue Ground to FE branch
4x GNDA		Power	Analogue Ground	0V Analogue Ground
4x AVDD		Power	Ext. Analogue Power	Ext. Power for Analogue
4x VDDA		Power	Reg. Analogue Power	Regulated Power for Analogue
DVSSA			ESD Return	0V Ground specific to ESD return
5x GNDD		Power	Digital Ground	0V Digital Ground
5x DVDD		Power	Ext. Digital Power	Ext. Power for Digital
5x VDDD		Power	Reg. Digital Power	Regulated Power for Digital
DVSS		Power	ESD Return	0V Ground specific to ESD return

Table 3-33: ABC130 Pads description

3.4.8 DC Supply and Control Characteristics:

The DC supply voltages requirements as defined below apply to the core of the ABC130 chip and will be delivered either from the internal on chip power management circuitry or from the external power sources via bond pads.

Table 3-34 : DC supply voltages

	Pad Name	Min	Nominal	Max	Absolute Max
Analogue Supply*	VDDA	1.15	1.2	1.25	1.6
Analogue Ground	GNDA		0		-0.3
Digital Supply#	VDDD	1.15	1.2	1.25	1.6
Digital Ground	GNDD		0		-0.3

* DC supplies are the one applied to the analogue circuits, from either an output source or from the internal analogue voltage regulator.

DC supplies are the one applied to the digital circuits, from either an output source or from the internal digital voltage regulator. For the on chip power-up reset to operate correctly the VDD power supply must be ramped up to 90% of its final value in less than 10 ms.

The current draw at each DC input is as follows (values excluding the regulators current).

Table 3-35 : DC supply currents for the nominal voltage supplies (VDDA=1.2V, VDDD=1.2V) and nominal operating conditions

		Min	Nominal	Max
Analogue Supply	VDDA		70mA	
Analogue Ground	GNDA			
Digital Supply*	VDDD		140mA	
Digital Ground	GNDD			

Table 3-36 : Absolute Min/Max current draws at power supply inputs which may occur in non-standard operating conditions, e.g. all bias DACs set at zero or to full range, clock not supplied to the chips

		Min	Nominal	Max
Analogue Supply	VDDA			
Digital Supply	VDDD			

3.4.9 Power Consumption

Expected typical power consumption for nominal bias power supply voltages and bias currents: <1 mW/channel.

3.4.10 Input/Output Levels

Table 3-37 : Input Levels for SLVS Inputs (Clock, BC, COM-L0, R3-L1)

Parameter	Conditions	Minimum	Maximum
Input Voltage Range Vi		0	Vdd
InputVoltage Common mode Vicm		0.2V	1.0V
Effective Input Offset	MC result	0V	+/-10mV
Common mode resistance to Vdd/2	Termination On	450 Ω	550 Ω
Receiver input impedance	Termination ON Termination OFF	75Ω >1Meg	82 Ω

Table 3-38 : Input Levels for special Inputs (Bidirectional Xoff, Data)

Parameter	Conditions	Minimum	Maximum
Input Voltage Range Vi		0	1.2V
InputVoltage Common mode Vicm		0.2V	1.0V
Input Offset	Monte Carlo Runs	0	+/-10mV
Common Mode Resistance to Vdd/2	Receive mode On	450 Ω	550 Ω
Receiver input impedance	Receive mode On	75 Ω	82 Ω

Table 3-39 : Output Levels for SLVS Outputs (Xoff, Data)

Parameter		Minimum	Maximum
Output Current	8 programmable steps	1mA	7mA
Output offset Voltage	Symmetric Drive		0

Output Differential Voltage	With 75 Ω Termination	75mV	520mV
Output impedance		k Ω	

3.4.11 Shunt and Voltage Regulators

The ABC130 chips can be supplied by a constant current source or a voltage source. With a current source, the supply voltages for the analogue and digital parts of the circuit are regulated by the shunt regulator controlled with the ShuntCtrl analogue signal that is part of an external feedback loop circuit. The internal supply voltages for the analogue or digital parts of the circuit are derived from the external voltages separately by two on-chip linear voltage regulators. The shunt regulator is disabled by pulling down the padShuntCtrl signal to GND. The linear voltage regulators can be disabled by pulling up the Disable_RegA and Disable_RegD inputs to AVDD. Pads are provided to eventually feed the power to the chip directly from outside, not using the regulations circuits.

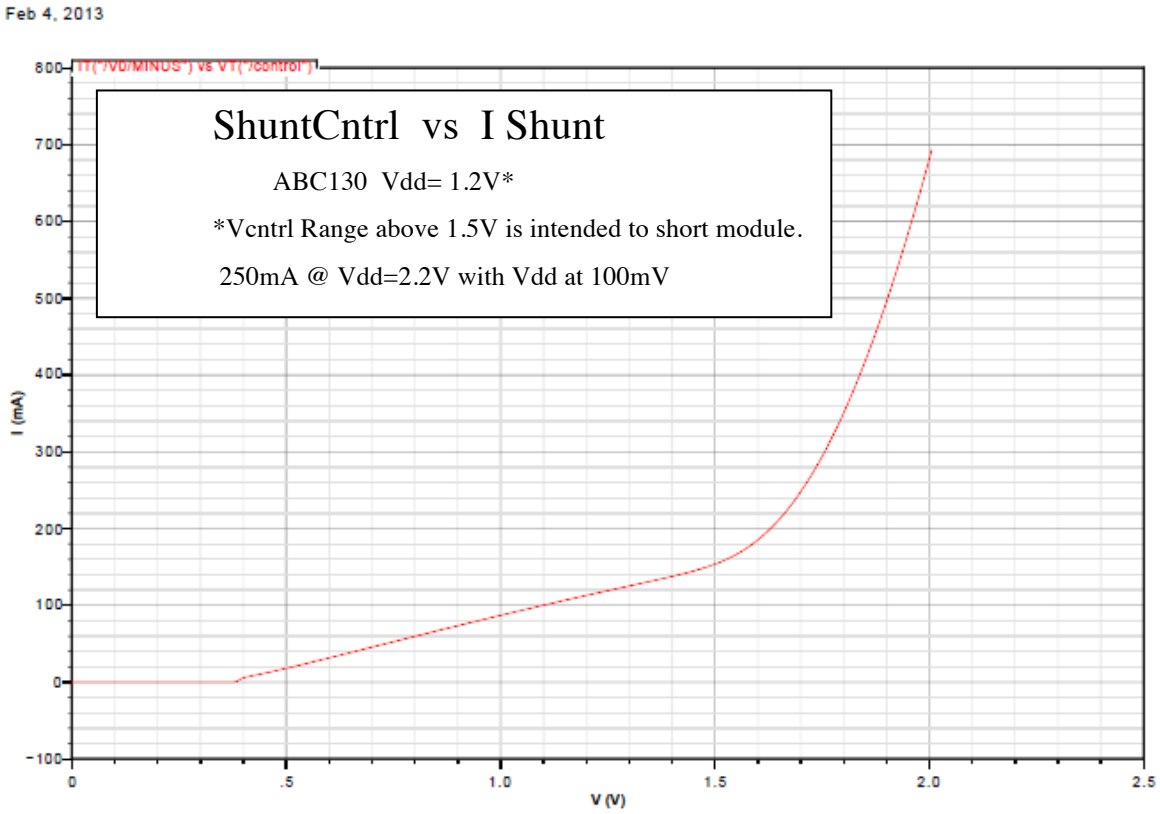
The shunt regulators must allow connecting their outputs in parallel on the hybrid even if the output voltages of the individual devices are not perfectly matched. It is required that devices with mismatch of output voltages within a range ±100 mV can be connected in parallel.

3.4.11.1 Shunt regulator

The shunt regulator is consisting of only the shunt power device. The input ShuntCtrl has to be connected to the feedback control circuitry outside of ABC130 to control it. The ABC130 Shunt block is intended to be controlled by the SPP ASIC that has a control range of up to 2.2V. If no control is provided, it is good practice to hard connect ShuntCtrl to GND, so that the shunt device cannot derive any current from the power supply.

Table 3-40 : Shunt regulator specifications

		Min	Nominal	Max
Minimum shunt current	Ishuntmin	1uA	30mA@ShuntCtrl=.6V	150mA@Shunt Ctrl= 1.5V
Internal shunt current limit	Ishuntlimit0	1uA	250mA@ShuntCTRL= 2.2V with Vdd= 0.1V	
Disable inputs	ShuntCtrl		GND	
Response Time (0-90%)	ShuntCntrl		75ns	



3.4.11.2 Voltage Regulators

		Min	Nominal	Max
Input Voltage	AVDD	1.25	1.5	1.6*
Output voltage	VDDA	1.15	1.2	1.25
Output current	IDDA		70mA	

Table 3-41 : Analogue voltage regulator specifications

The analogue voltage regulator provides the voltage to the front-end circuitry. It can be disabled by pulling up to AVDD the Disable_RegA input. In this case the front-end can be powered from an external voltage source connected to the analogue power pins VDDA and GNDA and GNDIT for the input branch).

* : 1.6V is the limit imposed by the technology reliability parameters. The regulator circuit has been proven to operate at higher VDD up to 2V (for short time).

		Min	Nominal	Max
Input Voltage	DVDD	1.25	1.5	1.6*
Output voltage	VDDD	1.15	1.2	1.25

Output current	IDDD		140mA	
Output Impedance			0.3 ohm	
Rejection Ratio				
Rejection Ratio with 100nF external capacitor				

Table 3-42 : Digital voltage regulator specification

The digital voltage regulator provides the voltage to the digital circuitry. It can be disabled by pulling up to AVDD the Disable_RegD input. In this case the digital part of the chip can be powered from an external voltage source connected to the digital power pins VDDD and GNDD.

* : 1.6V is the limit imposed by the technology reliability parameters. The regulator circuit has been proven to operate at higher VDD up to 2V (for short time).

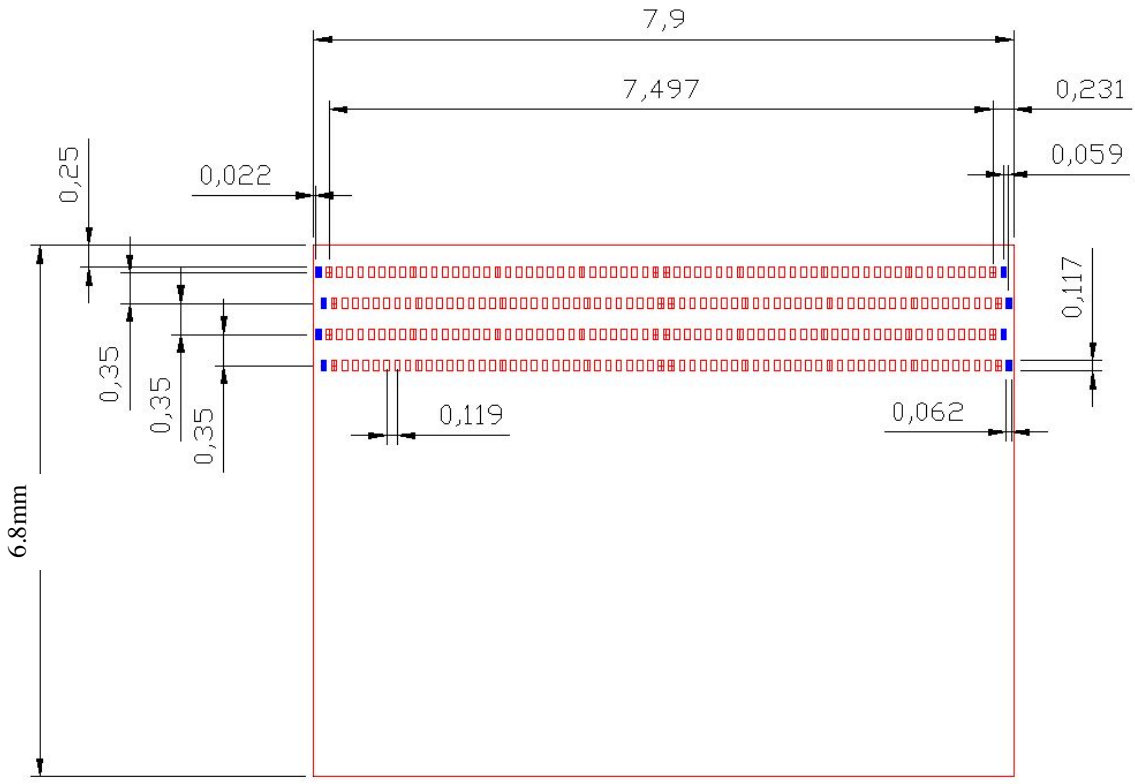
3.4.12 Physical Requirements

3.4.12.1 Floor plan

The ABC130 chip will be 7.9 mm wide and to fit at best the input pads to the sensor strip pitch, while keeping a reasonable gap between adjacent chips to allow the placement of decoupling capacitors.

The pad size opening are 95um by 190um in the “digital and power” section and 62um by 117um for the pads to the detector.

The front-end pads (to detector) are arranged as shown on Figure 3-10, in 4 rows of 64 pads with a pitch of 119um. For the detector reference GND (HV decoupling and guardring) there are 2x 4 pads on both sides of the staggered input pads.



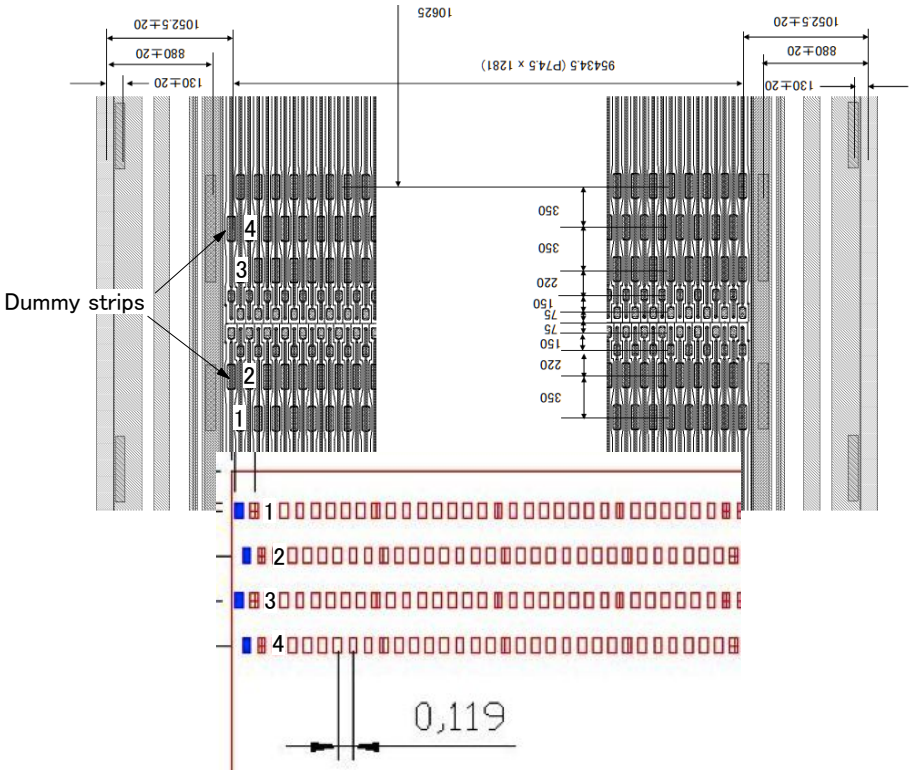


Figure 3-10 ABC130 detector pads arrangement

The other pads are approximately located as shown on Figure 3-11. The front-end pads are shown at the top, the right edge has SLVS inputs, the bottom side has the bidirectional transmission ports, the chip address and the power pads, the right side is populated with a few specific pads that do not need to be bonded on hybrids.

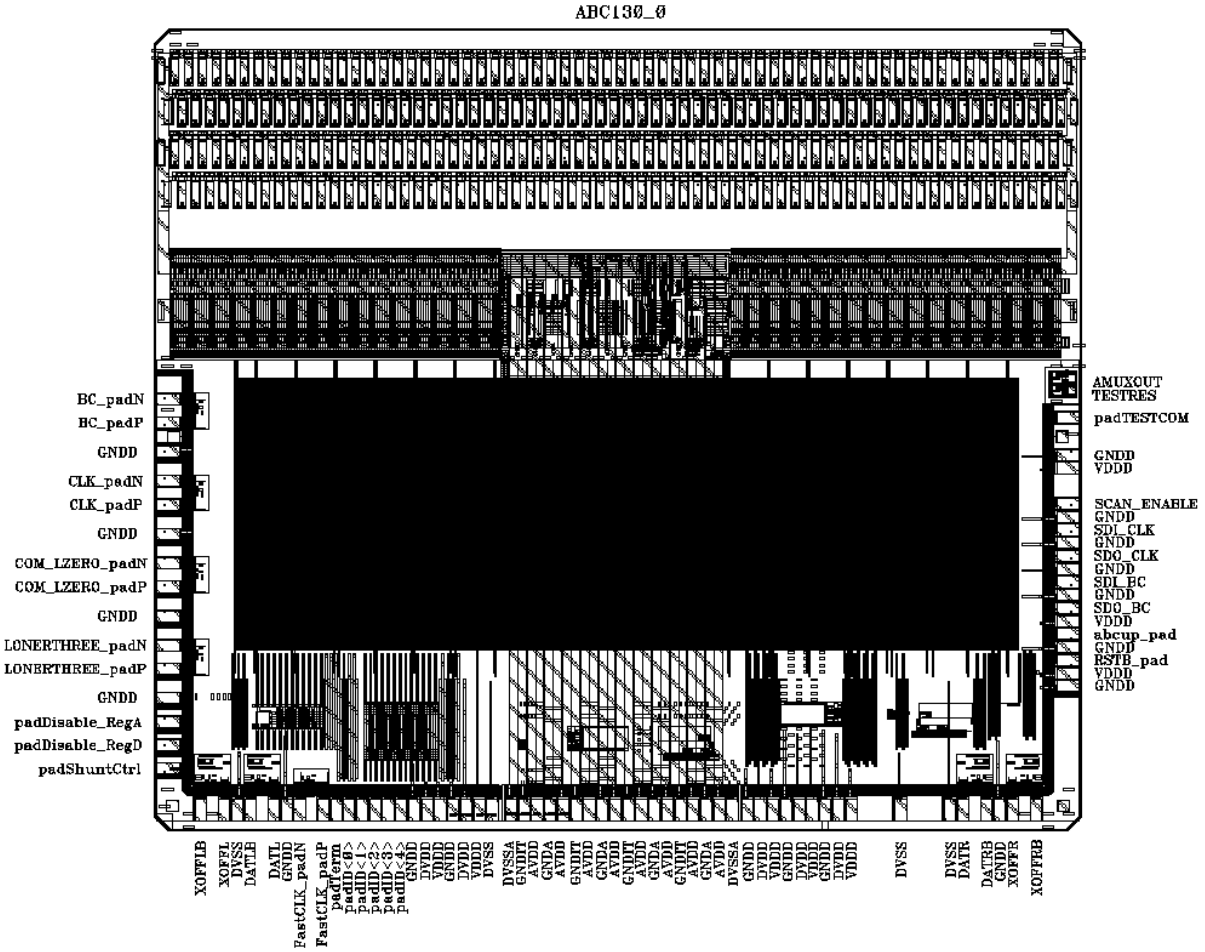


Figure 3-11 ABC130_0 Pads distribution

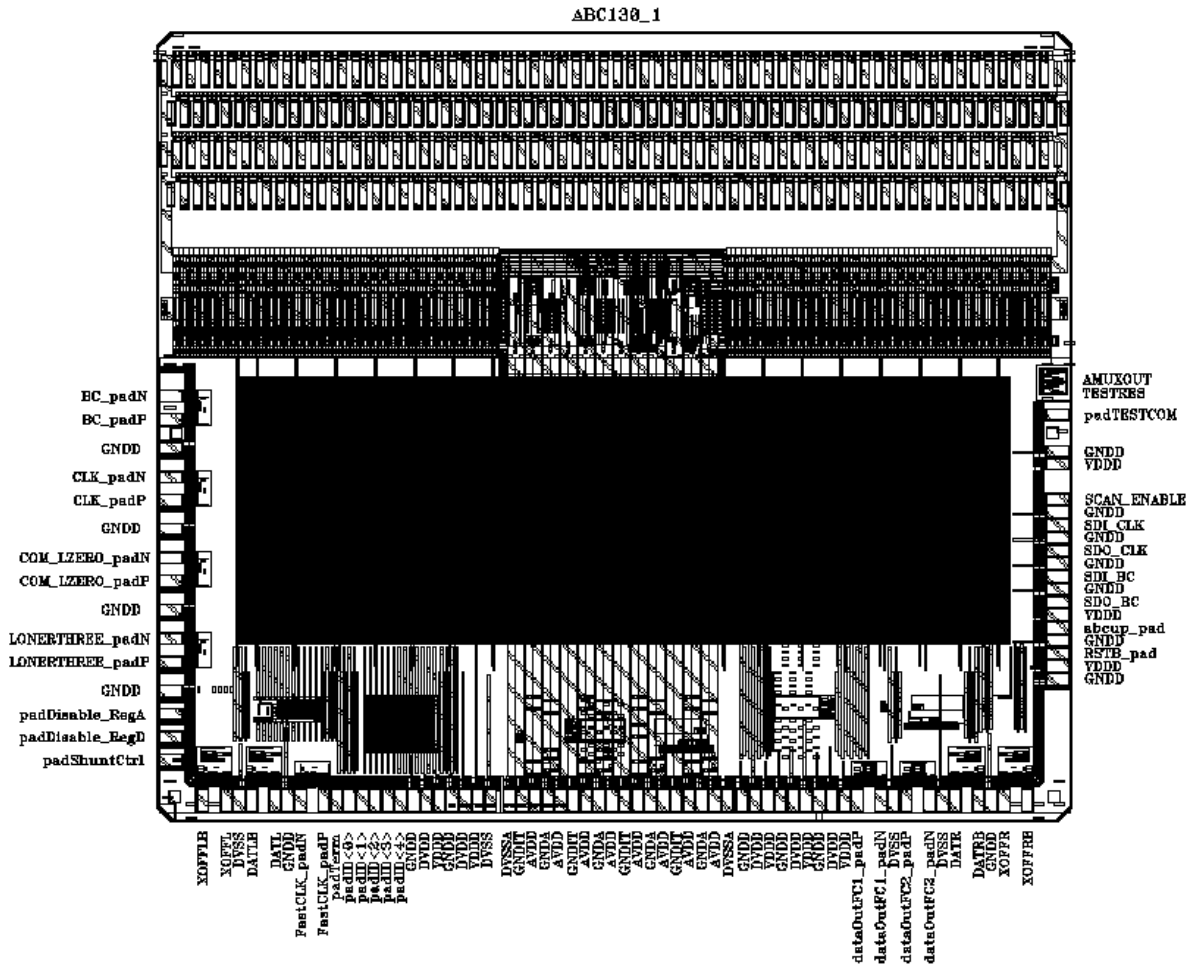


Figure 3-12 ABC130_1 Pads distribution