List of Publications
(as of May 2008)

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Book Chapters (1)

- T. Theocharides, C.A. Nicopoulos, K. Irick, N. Vijaykrishnan, and M. J. Irwin, **"An Exploration of Hardware Architectures for Face Detection,"** in the VLSI Handbook, Second Edition, CRC Press, Taylor & Francis Group, Chapter 83, 2007.

Journal Articles (3 + 4 to be submitted) (In reverse chronological order)

- F. Wang, C.A. Nicopoulos, X. Wu, Y. Xie, and N. Vijaykrishnan, **"Variation-aware Task and Communication Mapping for MPSoC Architectures,"** submitted to the IEEE Transactions on Very Large Scale Integration (TVLSI) Systems in February 2008.

- D. Park, C.A. Nicopoulos, J. Kim, N. Vijaykrishnan, and C.R. Das, **"Design Space Exploration for Fault-Tolerant On-Chip Interconnects,"** submitted to the IEEE Transactions on Dependable and Secure Computing (TDSC) in June 2007.

- C.A. Nicopoulos, S. Srinivasan, A. Yanamandra, D. Park, N. Vijaykrishnan, C.R. Das, and M.J. Irwin, **"On the Effects of Process Variation in Network-on-Chip Architectures,"** submitted to the IEEE Transactions on Dependable and Secure Computing (TDSC) in May 2007.

TO BE SUBMITTED:

- A. Cevrero, P. Athanasopoulos, H.P. Afshar, A.K. Verma, P. Brisk, F.K. Gurkaynak, C.A. Nicopoulos, Y. Leblebici, and P. Ienne, **"Architectural improvements for field programmable counter arrays: enabling efficient synthesis of fast compressor trees on FPGAs,"** to be submitted to the ACM Transactions on Reconfigurable Technology and Systems (TRETS).

- C.A. Nicopoulos, T.D. Richardson, D.Park, N. Vijaykrishnan, C.R. Das, and M.J. Irwin, **"Toward Scalable System-on-Chip Interconnection**

Networks," to be submitted to the IET Research Journal of Computers & Digital Techniques.

- J. Kim, C.A. Nicopoulos, D. Park, R. Das, Y. Xie, N. Vijaykrishnan, and C.R. Das, **"Cubical Router Design for On-Chip Communication in 3D Architectures,"** to be submitted to the IEEE Transactions on VLSI Systems (TVLSI).

- J. Kim, C.A. Nicopoulos, D. Park, N. Vijaykrishnan, M.S. Yousif, and C.R. Das, **"A Decomposable Router Architecture for Gracefully Degrading Network-on-Chip Design,"** to be submitted to the IEEE Transactions on Parallel and Distributed Systems (TPDS).

Conference Proceedings / Other (17 + 2 under submission) (In reverse chronol. order)

UNDER SUBMISSION:

- B. Raman, C.A. Nicopoulos, P. Thiran, and P. Ienne, **"Analytical Models of Communication in Multi-Processor Systems-on-Chip (MPSoC),"** under submission to the 29th IEEE Real-Time Systems Symposium (RTSS), submitted in May 2008.

- S. Hosein, A. Cevrero, P. Brisk, F.K. Gurkaynak, C.A. Nicopoulos, P. Ienne, and Y. Leblebici, **"Design Space Exploration for Field Programmable Counter Arrays,"** under submission to the 2008 International Conference on Compilers, Architecture, and Synthesis for Embedded Systems (CASES), submitted in April 2008.

PUBLISHED:

- N. Soundararajan, A. Yanamandra, C.A. Nicopoulos, N. Vijaykrishnan, A. Sivasubramaniam, and M.J. Irwin, **"Analysis and solutions to Issue Queue Process Variation,"** to appear in Proceedings of the International Conference on Dependable Systems and Networks (DSN), June 2008.

  [11 pages – *Premiere* conference in System Reliability – very competitive]

- R. Das, A.K. Mishra, C.A. Nicopoulos, D. Park, N. Vijaykrishnan, R. Iyer, M.S. Yousif, C.R. Das, **"Performance and Power Optimization through Data Compression in Network-on-Chip Architectures,"** in Proceedings of the 14th International Symposium on High-Performance Computer Architecture (HPCA), February 2008.

  [12 pages – *Premiere* conference in Computer Architecture – extremely competitive]

- C.A. Nicopoulos, A. Yanamandra, S. Srinivasan, N. Vijaykrishnan, and M.J. Irwin, **"Variation-Aware Low-Power Buffer Design,"** in Proceedings of the 41st Asilomar Conference on Signals, Systems, and Computers, pp. 1402-1406, 2007.

- F. Wang, C.A. Nicopoulos, X. Wu, Y. Xie, and N. Vijaykrishnan, **"Variation-aware Task Allocation and Scheduling for MPSoC,"** in

Proceedings of the International Conference on Computer-Aided Design (ICCAD), pp. 598-603, 2007.

[*Premiere* conference in Computer-Aided Design – very competitive]

- D. Park, R. Das, C.A. Nicopoulos, J. Kim, N. Vijaykrishnan, R. Iyer, and C. R. Das, **"Design of a Dynamic Priority-Based Fast Path Architecture for On-Chip Interconnects,"** in Proceedings of the 15th Hot Interconnects Symposium, pp. 15-20, 2007.

  [*Premiere* conference in Interconnect Architectures – very competitive]

- J. Kim, C.A. Nicopoulos, D. Park, R. Das, Y. Xie, N. Vijaykrishnan, and C.R. Das, **"A Novel Dimensionally-Decomposed Router for On-Chip Communication in 3D Architectures,"** in Proceedings of the 34th Annual International Symposium on Computer Architecture (ISCA), pp. 138-149, 2007.

  [12 pages – *Premiere* conference in Computer Architecture – extremely competitive]

- C.A. Nicopoulos, D. Park, J. Kim, N. Vijaykrishnan, M.S. Yousif, and C.R. Das, **"ViChaR: A Dynamic Virtual Channel Regulator for Network-on-Chip Routers,"** in Proceedings of the 39th Annual International Symposium on Microarchitecture (MICRO), pp. 333-344, 2006.

  [12 pages – *Premiere* conference in Computer Architecture – extremely competitive]

- D. Park, C.A. Nicopoulos, J. Kim, N. Vijaykrishnan, and C.R. Das, **"A Distributed Multi-Point Network Interface for Low-Latency, Deadlock-Free On-Chip Interconnects,"** in Proceedings (electronic) of the International Conference on Nano-Networks (Nano-Net), 2006.

- F. Li, C.A. Nicopoulos, T. Richardson, Y. Xie, N. Vijaykrishnan, and M. Kandemir, **"Design and Management of 3D Chip Multiprocessors Using Network-in-Memory,"** in Proceedings of the 33rd Annual International Symposium on Computer Architecture (ISCA), pp. 130-141, 2006.

  [12 pages – *Premiere* conference in Computer Architecture – extremely competitive]

- J. Kim, C.A. Nicopoulos, D. Park, N. Vijaykrishnan, M.S. Yousif, and C.R. Das, **"A Gracefully Degrading and Energy-Efficient Modular Router Architecture for On-Chip Networks,"** in Proceedings of the 33rd Annual International Symposium on Computer Architecture (ISCA), pp. 4-15, 2006.

  [12 pages – *Premiere* conference in Computer Architecture – extremely competitive]

- D. Park, C.A. Nicopoulos, J. Kim, N. Vijaykrishnan, and C.R. Das, **"Exploring Fault-Tolerant Network-on-Chip Architectures,"** in Proceedings of the International Conference on Dependable Systems and Networks (DSN), pp. 93-102, 2006.

  [10 pages – *Premiere* conference in System Reliability – very competitive]

- J. Kim, D. Park, C.A. Nicopoulos, N. Vijaykrishnan, and C.R. Das, **"Performance Enhancement through Early Release and Buffer Optimization in Network-on-Chip Router Architectures,"** in Special

Workshop on Future Interconnects and Networks on Chip at the Design, Automation and Test in Europe (DATE) Conference, 2006.

- T.D. Richardson, C.A. Nicopoulos, D. Park, N. Vijaykrishnan, Yuan Xie, C.R. Das, and V. Degalahal, **"A Hybrid SoC Interconnect with Dynamic TDMA-Based Transaction-Less Buses and On-Chip Networks,"** in Proceedings of the 19th International Conference on VLSI Design, pp. 657-664, 2006.

- J. Kim, C.A. Nicopoulos, D. Park, N. Vijaykrishnan, and C.R. Das, **"A Fine-Grained Modular Architecture for System-on-Chip Networks,"** Technical Report, CSE-06-013, Department of Computer Science and Engineering, The Pennsylvania State University, University Park, PA, 2006.

- J. Kim, D. Park, C.A. Nicopoulos, N. Vijaykrishnan, and C.R. Das, **"Design and analysis of an NoC architecture from performance, reliability and energy perspective,"** in Proceedings of the 1st Symposium on Architectures for Networking and Communications Systems (ANCS), pp. 173-182, 2005.

  [10 pages – New competitive conference in Communications Architectures]

- J. S. Kim, C.A. Nicopoulos, N. Vijaykrishnan, Y. Xie, and E. Lattanzi, **"A Probabilistic Model for Soft-Error Rate Estimation in Combinational Logic,"** in the 1st International Workshop on Probabilistic Analysis Techniques for Real Time and Embedded Systems (PARTES), 2004.

- C.A. Nicopoulos, **"Smart Antennas for Wireless Communications,"** Undergraduate Honors Thesis (under J.F. Doherty), Department of Electrical Engineering, The Pennsylvania State University, University Park, PA, 2003.