Curriculum Vitae

Chrysostomos A. Nicopoulos

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Personal Information

Work Address:

EPFL – IC – ISIM – LAP
INF 139
Station 14
CH-1015 Lausanne
Switzerland

Tel (Mobile): +41 78 897 44 40
Fax (Departmental): +41 21 69 35263

Email: ***chrys.nicopoulos@epfl.ch***
Webpage: ***www.nicopoulos.eu***

Cyprus Home Address:

24 Protis Apriliou Street
Lakatameia
CY-2310 Nicosia
Cyprus

Tel: +357 22 386628

Birth Date: 25 May 1977
Birth Place: Nicosia, Cyprus
Citizenship: Cypriot (*European Union Citizen*)

Education

August 2007 (Official Degree Conferral: *December 2007*)
Ph.D. in Electrical Engineering (Specialization in Computer Engineering)

- The Pennsylvania State University, University Park, PA 16802, USA
- Thesis Title: "**Network-on-Chip Architectures: A Holistic Design Exploration**"
- Thesis Adviser: Dr. Vijaykrishnan Narayanan
- GPA: 3.94/4.00

May 2003
B.Sc. in Electrical Engineering with Minor in Mathematics

- The Pennsylvania State University, University Park, PA 16802, USA
- **GPA: 4.00/4.00** – Dean's List throughout undergraduate studies
- **Ranked FIRST among 335 Electrical Engineering undergraduates**
- Graduated from the prestigious **Schreyer Honors College**, which oversees the Honors Program at Penn State. Took Honors versions of the core Electrical Engineering courses (more challenging, design- and research-based,

specifically designed for Honors Scholars), and submitted a **Final Year Honors Thesis** (in addition to the mandatory Senior Design Project).
- Honors Thesis Title: "Smart Antennas for Wireless Communications"

Research Interests

- High-performance, low-power, and fault-tolerant Network-on-Chip (NoC) router architectures for Chip Multi-Processors (CMP) and heterogeneous Multi-Processor Systems-on-Chip (MPSoC).
- Computer architecture.
- Three-dimensional (3D) system architectures.
- Communication-centric many-core computer architectures.
- On-chip network topologies.
- Application mapping to NoC-based designs.
- Performance evaluation of NoCs using workload traces.
- Digital systems design.
- Embedded systems design.
- High-performance, power-efficient and reliable VLSI architectures.
- Process Variation (PV)-aware VLSI design.
- Fault-tolerant System-on-Chip (SoC) design and integration.

Work/Research Experience

October 2007 – Present
Postdoctoral Research Associate

Ecole Polytechnique Federale de Lausanne (EPFL)
(Swiss Federal Institute of Technology, Lausanne)

La faculté Informatique & Communications
(I&C School of Computer and Communication Sciences)
Laboratoire d'Architecture de Processeurs (LAP)
(Processor Architecture Laboratory)

- Coordinator of a major research initiative at EPFL in 3D system architectures, involving three labs.
  - The project covers all aspects of 3D design: from low-level physical design, to architectural exploration, to system-level optimizations.
  - Responsibilities include organizing, assigning, and overseeing the various constituent sub-projects, and reporting the progress status to the three lab heads.

- Coordinator of a research project on on-chip non-uniform shared caches (NUCA architectures) in many-core CMPs.
  - The project – called Distributed Shared Caches (DiSC) and headed by Prof. Babak Falsafi – deals with issues pertaining to NUCA cache coherence protocols in the many-core chips of the near future.

In particular, the project investigates the notion of workload-aware coherence.

- The underlying on-chip interconnection backbone is designed in conjunction with the cache coherence schemes in order to achieve efficient and harmonious synergy between protocols and interconnects.

General Research in the areas of:

- Computer Architecture.
- Computer Engineering.
- Embedded Systems.
- Field Programmable Gate Arrays (FPGA).
- Field Programmable Counter Arrays (FPCA).
- Computer Arithmetic.
- Analytical Models of Communication in MPSoCs.

2003 – 2007
Graduate Research and Teaching Assistant

Research Experience (Conference where work appeared shown in square brackets)

Thesis-Related Doctoral Research:

- Research in high-performance, area- and power-efficient, and reliable NoC architectures.
- Developed an intelligent, path-sensitive router design, augmented with an array of algorithmic and microarchitectural techniques to safeguard against both link failures and intra-router upsets **[ANCS-05]**.
- Developed an ultra-low latency, fully decoupled modular router architecture, which degrades gracefully and provides high resilience against hard failures **[ISCA-06]**.
- Conducted extensive research into fault-tolerant NoC implementations and provided the first comprehensive analysis of the severity of intra-router soft errors **[DSN-06]**.
- Presented the *first* thorough exploration of the ramifications of process-variation-induced anomalies on the overall operation of the on-chip interconnection fabric, and provided appropriate microarchitectural solutions **[Asilomar-2007 and Journal Submitted to IEEE TDSC in May 2007]**.
- Developed a dynamic path management scheme that exploits prevailing network conditions to expedite the traversal of flits in frequently used paths by utilizing a reduced router pipeline **[Hot Interconnects 2007]**.
- Conducted the *first* in-depth study in integrating the network-on-chip paradigm into a three-dimensional circuit implementation of a shared L2 Non-Uniform Cache Access (NUCA) CMP structure **[ISCA-06]**.
- Presented the *first* detailed design-space exploration of three-dimensional NoC router architectures, and developed a dimensionally-decomposed router design to facilitate efficient interconnection in complex 3D chip structures **[ISCA-07]**.

- Investigated the benefits of real-time data compression within the on-chip network to reduce the number of in-flight packets, thereby improving network performance **[HPCA-2008]**.
- Developed a novel dynamic buffer manager for on-chip switches, which allows for the halving of buffer resources with no discernible effect on performance (yielding enormous area and power savings) **[MICRO-06]**.
- Developed a high-performance, dynamic Time-Division Multiple Access (dTDMA) bus architecture for on-chip communication, and investigated several hybrid NoC-Bus topologies for future MPSoCs and embedded systems **[VLSID-06]**.
- Conducted in-depth exploration and quantified the effects of data compression in on-chip networks within the context of NUCA in large-scale CMPs.
- Developed an inherently deadlock-free Multiple Entry Point (MEP) on-chip network interface and associated topology **[Nano-Net-06]**.
- Developed fault-tolerant and thermal-aware routing algorithms, and deadlock-recovery mechanisms for on-chip interconnection networks.
- Designed and implemented a Service-Oriented Networking (SON) scheme, which utilizes redundant computation resources in many-core systems to redirect on-chip traffic away from faulty nodes to alternative functional elements.
- Developed a queuing-theory-based analytical model for 2D mesh networks, which performs latency and power analysis at the granularity of individual router sub-modules for increased accuracy **[ANCS-05]**.
- Hardware design and synthesis of individual router components for use in parameterized architectural area and power NoC models (using commercial-grade tools and libraries).
- Design and development of cycle-accurate network simulation tools incorporating static and dynamic power estimation algorithms for architectural-level design-space exploration.
- Development of a 3D on-chip network simulator integrated with a full-system simulation environment for analysis of shared cache hierarchies in large CMPs.
- Development of an integrated, trace-driven NoC/cache simulation environment for studying the behavior of the interconnection network in NUCA CMP implementations.

Other Doctoral Research:

- Analyzed the impact of process variation on a microprocessor's issue queue and proposed various architectural solutions to guard against variability-induced effects **[DSN-08]**.
- Design, synthesis, physical placement and wire routing, simulation, and verification (i.e. complete ASIC design flow) of an embedded hardware face detection processor, implemented using a neural-network-based algorithm **[VLSI Handbook 2007, Chapter 83]**.
- Proposed a variation-aware task allocation and scheduling algorithm for Multiprocessor System-on-Chip (MPSoC) architectures to mitigate the impact of parameter variations **[ICCAD-07]**.

- Developed an analytical probabilistic model for the estimation of soft-error rates in combinational logic circuit blocks **[PARTES-04]**.

Teaching Experience

Teaching Assistant for the Senior Communication/Computer Networks Course (Undergraduate Level)

- Teaching assistant for four consecutive semesters (two academic years).
- In charge of the coursework portion of the course (i.e. preparation, setup and grading of projects and homework assignments).
- Assisted in the preparation of midterm and final examinations.
- Lectured some parts of the course as a substitute for the instructor.

2001 – 2003
Undergraduate Research Assistant

SPIRIT (Student Projects Involving Rocket Investigation Techniques) Program at Penn State

- NASA and private-industry-funded research program to build a rocket to carry out experiments in the mesosphere.
- Joined the Experiments Group in August 2001, and designed a circuit used to measure electron content/density in the mesosphere.
- Conducted pre-launch experiments at NASA Wallops Island Base, in Virginia, USA, under the guidance and supervision of several NASA engineers.
- Rocket was successfully launched on 3 October, 2003.

Undergraduate Honors Research

- In partial fulfillment of Undergraduate Honors Thesis.
- Performed research on smart antennas for wireless communications, under the supervision of Dr. John F. Doherty (Department of Electrical Engineering).
- Research involved extensive computer programming and simulation.

2000 (summer)
Application Developer and Network Administrator

CYTANET Internet Service Provider, Cyprus Telecommunications Authority (CYTA), Nicosia, Cyprus

- Set up and maintained Local and Wide Area Networks.
- Set up and maintained UNIX and Windows NT Servers, including special content servers, such as Streaming Audio/Video and WAP (Wireless Application Protocol) Servers.
- Participated in CISCO Systems router installation, configuration and maintenance.

1996 – 1998
Military Experience

Reserve Officer in the Armored Division of the Cyprus Army

- Attended a military academy for reserve officers in Athens, Greece, specializing in Main Battle Tanks.
- Served 26-month military service as an officer, managing four tanks and sixteen men as Commander of a Tank Platoon.
- Currently a reserve officer at the rank of Second Lieutenant.

Fellowships, Honors & Awards, and Professional Achievements

Awards

- Recipient of the *highly prestigious* Evan Pugh Scholar Award at Penn State in April 2003 **(Upper 0.5 percent of graduating class)**.
- Recipient of a College of Engineering **Graduate Fellowship** at Penn State in March 2003.
- Recipient of a 3-year **Graduate Fellowship** from the Electrical Engineering Department at Penn State in March 2003.
- Awarded a **Fulbright Scholarship** to study in the USA in 1998.
- Represented Cyprus in the World Debating and Public Speaking Championships in 1995.
- Member of the Cyprus Delegation in the European Youth Parliament's 1995 session in Gothenburg, Sweden.
- **Pan-Cyprian Champion** in the Toastmasters Public Speaking Competitions (in both Greek and English versions) in 1994.

Professional Certifications

- Recipient of the Technology Collaborative (formed after the merger of the Pittsburgh Digital Greenhouse and the Robotics Foundry) **Certificate in System-on-Chip Design**, May 2006.

Professional Affiliations

- Gigascale Systems Research Center (GSRC) Student Member, (http://www.gigascale.org/). {*2005 – 2007*}
- IEEE Student Member (plus IEEE Computer Society member). {*2006 – Present*}
- ACM Student Member (plus SIGARCH and SIGMICRO Special Interest Groups member). {*2006 – Present*}

Publications

Book Chapters (1)

- T. Theocharides, C.A. Nicopoulos, K. Irick, N. Vijaykrishnan, and M. J. Irwin, **"An Exploration of Hardware Architectures for Face Detection,"** in the VLSI Handbook, Second Edition, CRC Press, Taylor & Francis Group, Chapter 83, 2007.

Journal Articles (3 + 4 to be submitted) (In reverse chronological order)

- F. Wang, C.A. Nicopoulos, X. Wu, Y. Xie, and N. Vijaykrishnan, **"Variation-aware Task and Communication Mapping for MPSoC Architectures,"** submitted to the IEEE Transactions on Very Large Scale Integration (TVLSI) Systems in February 2008.

- D. Park, C.A. Nicopoulos, J. Kim, N. Vijaykrishnan, and C.R. Das, **"Design Space Exploration for Fault-Tolerant On-Chip Interconnects,"** submitted to the IEEE Transactions on Dependable and Secure Computing (TDSC) in June 2007.

- C.A. Nicopoulos, S. Srinivasan, A. Yanamandra, D. Park, N. Vijaykrishnan, C.R. Das, and M.J. Irwin, **"On the Effects of Process Variation in Network-on-Chip Architectures,"** submitted to the IEEE Transactions on Dependable and Secure Computing (TDSC) in May 2007.

TO BE SUBMITTED:

- A. Cevrero, P. Athanasopoulos, H.P. Afshar, A.K. Verma, P. Brisk, F.K. Gurkaynak, C.A. Nicopoulos, Y. Leblebici, and P. Ienne, **"Architectural improvements for field programmable counter arrays: enabling efficient synthesis of fast compressor trees on FPGAs,"** to be submitted to the ACM Transactions on Reconfigurable Technology and Systems (TRETS).

- C.A. Nicopoulos, T.D. Richardson, D.Park, N. Vijaykrishnan, C.R. Das, and M.J. Irwin, **"Toward Scalable System-on-Chip Interconnection Networks,"** to be submitted to the IET Research Journal of Computers & Digital Techniques.

- J. Kim, C.A. Nicopoulos, D. Park, R. Das, Y. Xie, N. Vijaykrishnan, and C.R. Das, **"Cubical Router Design for On-Chip Communication in 3D Architectures,"** to be submitted to the IEEE Transactions on VLSI Systems (TVLSI).

- J. Kim, C.A. Nicopoulos, D. Park, N. Vijaykrishnan, M.S. Yousif, and C.R. Das, **"A Decomposable Router Architecture for Gracefully Degrading Network-on-Chip Design,"** to be submitted to the IEEE Transactions on Parallel and Distributed Systems (TPDS).

Conference Proceedings / Other (17 + 2 under submission) (In reverse chronological order)

UNDER SUBMISSION:

- B. Raman, C.A. Nicopoulos, P. Thiran, and P. Ienne, **"Analytical Models of Communication in Multi-Processor Systems-on-Chip (MPSoC),"** under submission to the 29th IEEE Real-Time Systems Symposium (RTSS), submitted in May 2008.

- S. Hosein, A. Cevrero, P. Brisk, F.K. Gurkaynak, C.A. Nicopoulos, P. Ienne, and Y. Leblebici, **"Design Space Exploration for Field Programmable Counter Arrays,"** under submission to the 2008 International Conference on Compilers, Architecture, and Synthesis for Embedded Systems (CASES), submitted in April 2008.

PUBLISHED:

- N. Soundararajan, A. Yanamandra, C.A. Nicopoulos, N. Vijaykrishnan, A. Sivasubramaniam, and M.J. Irwin, **"Analysis and solutions to Issue Queue Process Variation,"** to appear in Proceedings of the International Conference on Dependable Systems and Networks (DSN), June 2008.

  [11 pages – *Premiere* conference in System Reliability – very competitive]

- R. Das, A.K. Mishra, C.A. Nicopoulos, D. Park, N. Vijaykrishnan, R. Iyer, M.S. Yousif, C.R. Das, **"Performance and Power Optimization through Data Compression in Network-on-Chip Architectures,"** in Proceedings of the 14th International Symposium on High-Performance Computer Architecture (HPCA), February 2008.

  [12 pages – *Premiere* conference in Computer Architecture – extremely competitive]

- C.A. Nicopoulos, A. Yanamandra, S. Srinivasan, N. Vijaykrishnan, and M.J. Irwin, **"Variation-Aware Low-Power Buffer Design,"** in Proceedings of the 41st Asilomar Conference on Signals, Systems, and Computers, pp. 1402-1406, 2007.

- F. Wang, C.A. Nicopoulos, X. Wu, Y. Xie, and N. Vijaykrishnan, **"Variation-aware Task Allocation and Scheduling for MPSoC,"** in Proceedings of the International Conference on Computer-Aided Design (ICCAD), pp. 598-603, 2007.

  [*Premiere* conference in Computer-Aided Design – very competitive]

- D. Park, R. Das, C.A. Nicopoulos, J. Kim, N. Vijaykrishnan, R. Iyer, and C. R. Das, **"Design of a Dynamic Priority-Based Fast Path Architecture for On-Chip Interconnects,"** in Proceedings of the 15th Hot Interconnects Symposium, pp. 15-20, 2007.

  [*Premiere* conference in Interconnect Architectures – very competitive]

- J. Kim, C.A. Nicopoulos, D. Park, R. Das, Y. Xie, N. Vijaykrishnan, and C.R. Das, **"A Novel Dimensionally-Decomposed Router for On-Chip**

Communication in 3D Architectures," in Proceedings of the 34th Annual International Symposium on Computer Architecture (ISCA), pp. 138-149, 2007.

[12 pages – *Premiere* conference in Computer Architecture – extremely competitive]

- C.A. Nicopoulos, D. Park, J. Kim, N. Vijaykrishnan, M.S. Yousif, and C.R. Das, **"ViChaR: A Dynamic Virtual Channel Regulator for Network-on-Chip Routers,"** in Proceedings of the 39th Annual International Symposium on Microarchitecture (MICRO), pp. 333-344, 2006.

  [12 pages – *Premiere* conference in Computer Architecture – extremely competitive]

- D. Park, C.A. Nicopoulos, J. Kim, N. Vijaykrishnan, and C.R. Das, **"A Distributed Multi-Point Network Interface for Low-Latency, Deadlock-Free On-Chip Interconnects,"** in Proceedings (electronic) of the International Conference on Nano-Networks (Nano-Net), 2006.

- F. Li, C.A. Nicopoulos, T. Richardson, Y. Xie, N. Vijaykrishnan, and M. Kandemir, **"Design and Management of 3D Chip Multiprocessors Using Network-in-Memory,"** in Proceedings of the 33rd Annual International Symposium on Computer Architecture (ISCA), pp. 130-141, 2006.

  [12 pages – *Premiere* conference in Computer Architecture – extremely competitive]

- J. Kim, C.A. Nicopoulos, D. Park, N. Vijaykrishnan, M.S. Yousif, and C.R. Das, **"A Gracefully Degrading and Energy-Efficient Modular Router Architecture for On-Chip Networks,"** in Proceedings of the 33rd Annual International Symposium on Computer Architecture (ISCA), pp. 4-15, 2006.

  [12 pages – *Premiere* conference in Computer Architecture – extremely competitive]

- D. Park, C.A. Nicopoulos, J. Kim, N. Vijaykrishnan, and C.R. Das, **"Exploring Fault-Tolerant Network-on-Chip Architectures,"** in Proceedings of the International Conference on Dependable Systems and Networks (DSN), pp. 93-102, 2006.

  [10 pages – *Premiere* conference in System Reliability – very competitive]

- J. Kim, D. Park, C.A. Nicopoulos, N. Vijaykrishnan, and C.R. Das, **"Performance Enhancement through Early Release and Buffer Optimization in Network-on-Chip Router Architectures,"** in Special Workshop on Future Interconnects and Networks on Chip at the Design, Automation and Test in Europe (DATE) Conference, 2006.

- T.D. Richardson, C.A. Nicopoulos, D. Park, N. Vijaykrishnan, Yuan Xie, C.R. Das, and V. Degalahal, **"A Hybrid SoC Interconnect with Dynamic TDMA-Based Transaction-Less Buses and On-Chip Networks,"** in Proceedings of the 19th International Conference on VLSI Design, pp. 657-664, 2006.

- J. Kim, C.A. Nicopoulos, D. Park, N. Vijaykrishnan, and C.R. Das, **"A Fine-Grained Modular Architecture for System-on-Chip Networks,"** Technical

Report, CSE-06-013, Department of Computer Science and Engineering, The Pennsylvania State University, University Park, PA, 2006.

- J. Kim, D. Park, C.A. Nicopoulos, N. Vijaykrishnan, and C.R. Das, **"Design and analysis of an NoC architecture from performance, reliability and energy perspective,"** in Proceedings of the 1st Symposium on Architectures for Networking and Communications Systems (ANCS), pp. 173-182, 2005.

  [10 pages – New competitive conference in Communications Architectures]

- J. S. Kim, C.A. Nicopoulos, N. Vijaykrishnan, Y. Xie, and E. Lattanzi, **"A Probabilistic Model for Soft-Error Rate Estimation in Combinational Logic,"** in the 1st International Workshop on Probabilistic Analysis Techniques for Real Time and Embedded Systems (PARTES), 2004.

- C.A. Nicopoulos, **"Smart Antennas for Wireless Communications,"** Undergraduate Honors Thesis (under J.F. Doherty), Department of Electrical Engineering, The Pennsylvania State University, University Park, PA, 2003.

Oral Presentations

- **"ViChaR: A Dynamic Virtual Channel Regulator and Unified Buffer Structure for On-Chip Routers,"** Focus Center Research Program (FCRP) e-Connect Seminar (Given to eminent semiconductor industry sponsors by top US research institutions – very competitive presenter selection process), April 2007.
- **"3D + NoC: An Emerging Interconnect Paradigm,"** at Intel Corporation, Hillsboro, Oregon, USA, March 2007.
- **"ViChaR: A Dynamic Virtual Channel Regulator for Network-on-Chip Routers,"** at the 39th Annual International Symposium on Microarchitecture (MICRO), Orlando, Florida, USA, December 2006.
- **"Architectural Exploration in NoC Design,"** at the 2006 GSRC Annual Symposium, San Jose, California, USA, September 2006.
- **"A Novel Decomposable Router Architecture for On-Chip Networks,"** Guest Lecture at Graduate Seminar of the Department of Electrical & Computer Engineering, University of Cyprus, Nicosia, Cyprus, September 2006.
- **"A Gracefully Degrading and Energy-Efficient Modular Router Architecture for On-Chip Networks,"** at the 33rd Annual International Symposium on Computer Architecture (ISCA), Boston, Massachusetts, USA, June 2006.
- **"A 3D Network-on-Chip Simulator,"** at the GSRC Quarterly Workshop, Berkeley, California, USA, March 2006.
- **"HS3d: Hot Spot 3d,"** at the GSRC Quarterly Workshop, Berkeley, California, USA, March 2006.

Manuscript Reviews

- IEEE Transactions on Computers **(TC)**, IEEE Transactions on Parallel and Distributed Systems **(TPDS)**, IEEE Transactions on VLSI **(TVLSI)**, IEEE Transactions on Computer Aided Design **(TCAD)**, ACM Transactions on Architecture and Code Optimization **(TACO)**, International Conference on Architectural Support for Programming Languages and Operating Systems **(ASPLOS)**, Annual IEEE/ACM International Symposium on Microarchitecture **(MICRO)**, International Symposium on High-Performance Computer Architecture **(HPCA)**, IEEE/ACM Design Automation and Test in Europe Conference **(DATE)**, International Symposium on Low Power Electronics and Design **(ISLPED)**, International Conference on Computer-Aided Design **(ICCAD)**, International Symposium on Networks-on-Chip, International Conference on VLSI Design (VLSID), International Symposium on VLSI (ISVLSI), International Conference on Field Programmable Logic and Applications (FPL), IEEE Workshop on Signal Processing Systems (SiPS), International Conference on Nano-Networks (Nano-Net), International Conference on Communications, Circuits and Systems (ICCCAS), Workshop on Chip Multiprocessor Memory Systems and Interconnects (CMP-MSI).

References

Primary Referees (to provide Letters of Recommendation)

- **Dr. Vijaykrishnan Narayanan (Thesis Adviser)**
  Professor
  Department of Computer Science and Engineering
  The Pennsylvania State University, University Park, PA 16802, USA
  vijay@cse.psu.edu
- **Dr. Chita R. Das**
  Professor
  Department of Computer Science and Engineering
  The Pennsylvania State University, University Park, PA 16802, USA
  das@cse.psu.edu
- **Dr. Mary Jane Irwin**
  Professor (Evan Pugh Professor and A. Robert Noll Chair of Engineering)
  Department of Computer Science and Engineering
  The Pennsylvania State University, University Park, PA 16802, USA
  mji@cse.psu.edu

Postdoctoral Research Supervisor at EPFL, Switzerland (October 2007 – Present) (Also to provide Letter of Recommendation)

- **Dr. Paolo Ienne (Director of the Processor Architecture Laboratory)**
  Professor
  Laboratoire d'Architecture de Processeurs (LAP)
  (Processor Architecture Laboratory)

La faculté Informatique & Communications
(I&C School of Computer and Communication Sciences)
Ecole Polytechnique Federale de Lausanne (EPFL),
CH-1015 Lausanne, Switzerland
Paolo.Ienne@epfl.ch

Other Ph.D. Committee Members

- **Dr. Ken Jenkins**
  Professor and Department Head
  Department of Electrical Engineering
  The Pennsylvania State University, University Park, PA 16802, USA
  jenkins@engr.psu.edu
- **Dr. Ram Narayanan**
  Professor
  Department of Electrical Engineering
  The Pennsylvania State University, University Park, PA 16802, USA
  ram@ee.psu.edu
- **Dr. Paul S. Weiss (External Committee Member)**
  Distinguished Professor
  Departments of Chemistry and Physics
  The Pennsylvania State University, University Park, PA 16802, USA
  stm@psu.edu