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Hysteresis-free operation of suspended carbon nanotube transistors

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Abstract

Single-walled carbon nanotubes offer high sensitivity and very low power consumption when used as field-effect transistors in nanosensors[1, 2]. Suspending nanotubes between pairs of contacts, rather than attaching them to a surface, has many advantages in chemical[3], optical[4] or displacement[1, 5] sensing applications, as well as for resonant electromechanical systems[6, 7]. Suspended nanotubes can be integrated into devices after nanotube growth[3, 5, 8, 9], but contamination caused by the accompanying additional process steps can change device properties. Ultraclean suspended nanotubes can also be grown between existing device contacts[1, 4, 10, 11], but high growth temperatures limit the choice of metals that can be used as contacts. Moreover, when operated in ambient conditions, devices fabricated by either the post- or pre-growth approach typically exhibit gate hysteresis[3, 8, 10, 12], which makes device behaviour less reproducible. Here, we report the operation of nanotube transistors in a humid atmosphere without hysteresis. Suspended, individual and ultraclean nanotubes are grown directly between unmetallized device contacts, onto which palladium is then evaporated through self-aligned on-chip shadow masks. This yields pairs of needle-shaped source/drain contacts that have been theoretically shown to allow high nanotube–gate coupling and low gate voltages[13]. This process paves the way for creating ultrasensitive nanosensors based on pristine suspended nanotubes.

Subject terms: Carbon nanotubes and fullerenes Electronic properties and devices Synthesis and processing

Main

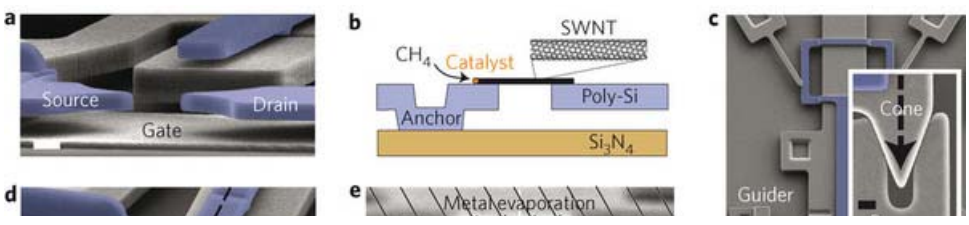
Sensors in which the nanotube channel of a field-effect transistor (FET) is suspended between two contacts have a number of advantages over those in which the FET nanotube adheres to a substrate. In particular, this arrangement allows free motion of the doubly-clamped nanotubes, which is useful when they are applied in flexural resonators and large-strain piezoresistive gauges. Moreover, avoiding contact between the nanotube and the substrate can attenuate low-frequency noise[14], reduce gate hysteresis[15] and result in larger active sensing areas. A useful feature is that the resonance frequency of the suspended nanotubes can be tuned by applying strain[16], which suggests that their integration into microelectromechanical systems (MEMS) actuators could give rise to novel applications.

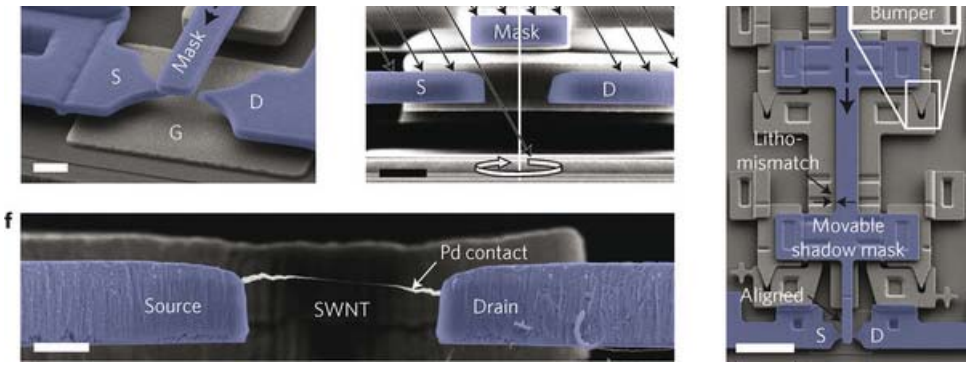
To date, two main methods have been used to fabricate devices that incorporate suspended nanotubes. After growth, the nanotubes can be suspended by using resist-based lithography, followed by metal deposition, lift-off and final release etch[5, 8, 9]. However, the resist contaminates the nanotubes, and the complete removal of organic resist residues is challenging, mainly because the necessary aggressive cleaning causes damage to the nanotubes. The other approach is to use a catalytic chemical vapour deposition (CVD) process to synthesize the nanotubes on top of the contacts. Although this avoids contamination arising from post-growth processes, the contact material must be able to withstand the high temperatures required for growing the nanotubes[1, 10, 11]. Moreover, the presence of H_2 in the CVD process can lead to the formation of metal hydrides, which prohibits the use of palladium, a favoured contact material, which swells substantially upon H_2 uptake.

Here, we propose an alternative method for the integration of suspended ultraclean nanotube FETs into prefabricated MEMS structures. In this, the use of movable on-chip micrometre-sized shadow masks to perform stencil lithography allows a wide range of metals to be used as contacts, without the need for any post-metallization treatment.

The approach for integrating single-walled carbon nanotubes (SWNTs) into suspended MEMS structures begins with predefined tip pairs made of polycrystalline silicon (poly-Si) fabricated by standard surface micromachining (Fig. 1a). The opposing tips comprising the source and drain are spaced 3 μm apart and are bridged by a suspended SWNT acting as a transistor gated by the substrate. The SWNTs are grown from patterned islands (see Methods) of size-separated catalysts[17] to span the gap between the tips, as shown in Fig. 1b. The nanotubes are oriented according to nearest-neighbour alignment[18]. Directly after growth, a guided on-chip shadow mask (Fig. 1c) is slid (see Methods) above the source and drain support tips so as to lie close to 800 nm above them (Fig. 1d). This mask shields the suspended middle section of the SWNT from metal deposition (Fig. 1e). By defining the mask and the tips in the same lithography step (see Methods), and by using the alignment cones built into the slider structure (inset of Fig. 1c), alignment of the shadow mask along the SWNT can be routinely achieved with an accuracy of less than 50 nm. All edges of the SWNT supporting structures are separated from the Si_3N_4-covered substrate by undercuts to maintain electrical isolation while subject to directional metal evaporation (Supplementary Fig. S1). Physical vapour deposition (PVD) is performed by electron-beam evaporation. Palladium is the preferred material[19] with which to contact SWNTs because of its high workfunction and good wetting properties. Small gaps between the shadow masks and suspended SWNTs (Fig. 1e) result in high material contrast (Supplementary Fig. S2). By rotating the samples about an axis with 30° tilt with respect to the material flux during evaporation (Fig. 1e), the electrode material thickness is gradually reduced towards the shadowed area. Consequently, tapered needle-type metal electrodes can be fabricated (Fig. 1f).

Figure 1: Contactless patterned metallization of suspended SWNTs by on-chip shadow masking.

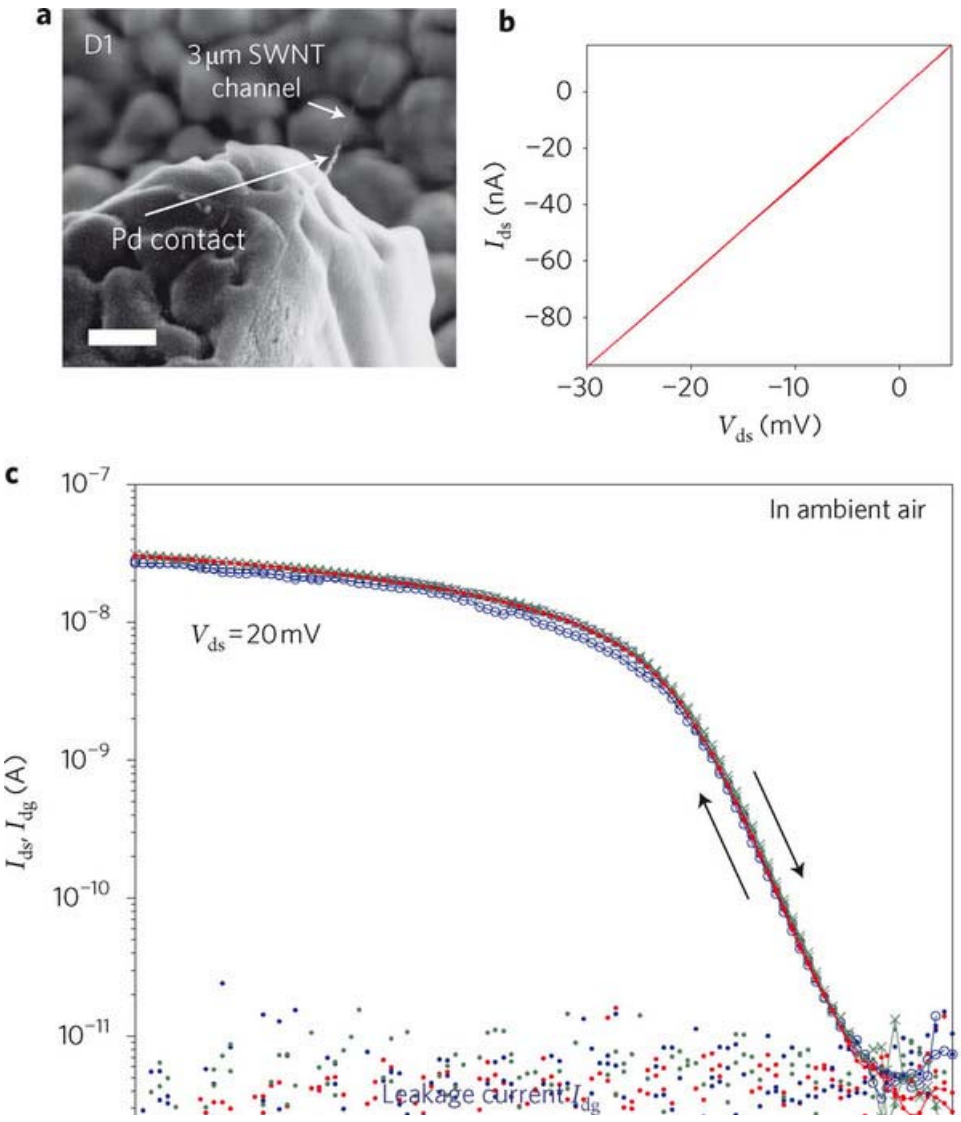


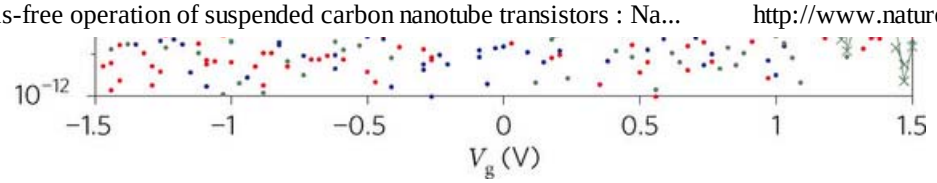


a, Scanning electron microscopy (SEM) image of the field-effect transistor architecture, showing the poly-Si support electrodes as source and drain (artificially coloured in blue). **b**, Schematic of a SWNT grown across opposing poly-Si tips. **c**, By moving (dashed arrows) the previously fully released slider from its initially retracted position, the on-chip shadow mask is placed closely above the part of the SWNT suspended between the source (S) and drain (D). Inset: cone, allowing for precise positioning. Alignment of the shadow mask to the tips is not affected by any mismatch between different photolithographic layers, because the mask and tips belong to the same layer (blue). **d**, Shadow mask in position. **e**, Front side view (SEM) of the opposing tips and shadow mask, including a schematic of tilted metal evaporation with sample rotation (white axis). The metal is patterned in a contactless manner to form electrical contacts with the SWNT. Undercuts act as intrinsic shadow masks and isolate the electrodes (S and D) from the substrate. **f**, On-chip shadow-masked evaporation of 170 nm palladium at a rotation axis tilted at 30° provides gradually thinned contacts with the free-standing SWNT and sidewall coverage. Scale bars: 2 μm (**a**); 25 μm, inset 2 μm (**c**); 5 μm (**d**); 2 μm (**e**); 1 μm (**f**).

Electrical device characterization was carried out at room temperature in ambient air. Figure 2a shows a long channel device (D1) with a channel length of 3 μm, suitable for strain or chemical sensing, and fabricated with a small gap of 1 μm between the shadow mask and the SWNT. The linear source–drain current (I_{ds}) versus source–drain voltage (V_{ds}) characteristic of device D1 at a gate voltage V_g = 0 V is shown in Fig. 2b, and I_{ds}–V_g curves for several V_g sweeps at 4 mV s^{-1} are plotted in Fig. 2c, showing repeatable FET behaviour. V_g was applied at the metallized backgate, 3 μm from the channel. The following device performance figures were determined: subthreshold swing S = 230 mV dec^{-1}, threshold voltage V_{th} = 1 V, on-state system resistance R_{on} = 330 kΩ and current on/off ratio I_{ds_on}/I_{ds_off} >1 × 10^4 at V_{ds} = 20 mV. The hysteresis in gate voltage was as low as 8 ± 5 mV and the hysteresis in current was 0.09 ± 0.06 nA, which corresponds to 0.3% of I_{ds_on}. Although difficult to compare directly due to its dependence on gate voltage range and scan rate, we note that hysteresis in ambient air is usually of the order of volts[3, 12].

Figure 2: Suspended, pristine SWNT arranged as a long-channel field-effect transistor with minute hysteresis.

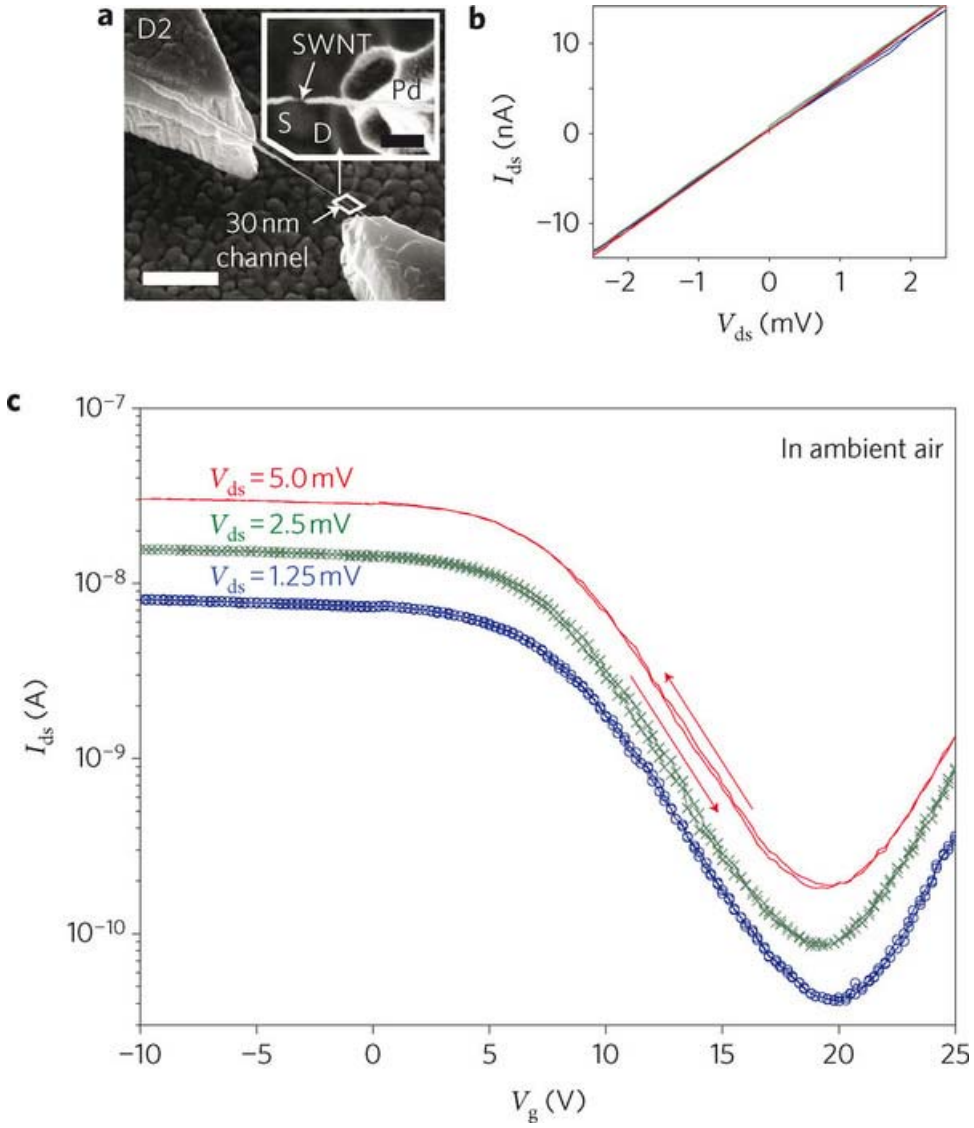




a, SEM micrograph of a SWNT contacted by on-chip shadow-masking with tilted-axis sample rotation during evaporation of 170 nm palladium (device D1, with a channel length of 3 μm). Scale bar, 200 nm. **b**, Source–drain current (I_{ds}) versus source–drain voltage (V_{ds}) curve for a gate voltage (V_g) of 0 V. **c**, I_{ds} versus V_g. Three dual sweeps (4 mV s^{-1}) are plotted for V_{ds} = 20 mV. The distance between the SWNT and backgate is 3 μm. Leakage current (I_{dg}) is at the level of noise. Note the negligibly small hysteresis.

By using a tilted sample rotation during palladium evaporation, the relatively large separation between the SWNT and the shadow mask allows very short non-metallized parts of the SWNT to occur. Short channel lengths as narrow as 30 nm could therefore be obtained (D2 in Fig 3a). The width of the shadow mask, the separation between the SWNT and mask, and the evaporation tilt angle may therefore be used as tuning parameters for the channel length and mechanical anchoring. The linear I_{ds}–V_{ds} characteristic of D2 is shown in Fig. 3b, and was found to withstand the FET measurements unchanged. I_{ds}–V_g curves are plotted in Fig. 3c. Even in an ambient cleanroom environment with 45% humidity, hysteresis was absent. To our knowledge, hysteresis is commonly observed for unpassivated channels exposed to humid air[3, 12], at least in approximately 50% of devices[20], unless the supporting surface is rendered hydrophobic[21]. For device D2, the following performance data were extracted: $S \approx 4{,}900$ mV dec^{-1}, V_{th} = 17 V with the backgate located 3 μm away from the channel, R_{on} = 89 kΩ and I_{ds_on}/I_{ds_off} = 190 at V_{ds} = 1.25 mV. Gate leakage current was below 2 × 10^{-11} A at I_{off}. The ambipolar FET behaviour can be attributed to ohmic palladium–SWNT contacts to a small-bandgap nanotube or to a large-diameter nanotube with moderate bandgap.

Figure 3: Suspended short-channel field-effect transistor without hysteresis.

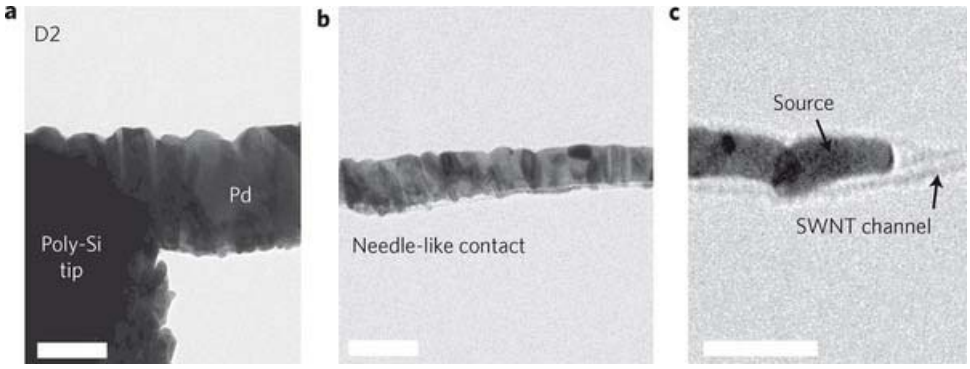


a, SEM image of a SWNT formed with an enlarged SWNT–shadow-mask gap, leading to a 30 nm short SWNT channel (device D2). Inset: enlargement of the channel (top view). Scale bars, 1 μm and 100 nm (inset). **b**, I_{ds}–V_{ds} curves at V_g = 0 V before and after FET measurements. **c**, I_{ds} measurements for the suspended directly contacted SWNT for continuous gate sweeps (0.3125 V s^{-1}) applied to the backgate (3 μm below the SWNT). Dual sweeps are shown for V_{ds} = 1.25, 2.5 and 5.0 mV. Note the absence of hysteresis.

Figure 4 shows the nanotapered contact of D2, recorded using transmission electron microscopy (TEM) under tilted-view conditions[22], allowing the combination

of electrical and structural characterization that is necessary for fundamental investigations and model validation. To avoid beam-induced defects or contamination, electron microscopy was conducted following electrical measurements. A bandgap of ~0.2 eV would be expected for the observed SWNT diameter of ~4 nm. The outermost metal contact diameter of D2 is ~7 nm (Fig. 4c).

Figure 4: Needle-like contacts for suspended as-grown SWNTs created by on-chip shadow masking.



a,**b**, TEM images of the gradual reduction in thickness of the evaporated palladium contact along the suspended SWNT of device D2 (Fig. 3). **c**, Close-up of the carbon nanotube FET channel, showing a nanoscale needle-like contact. Vibrations have caused image blurring. Scale bars: 50 nm (**a**); 50 nm (**b**); 25 nm (**c**).

Stencil lithography offers the possibility of contactless metal patterning, free of wet chemistry. The on-chip shadow masks used here allow for improved accuracy of alignment (within 50 nm) compared to off-chip wafer stencils, which is crucial for nanotube integration. In a feature that is important for this accuracy of alignment, as well as making use of the cone-and-bumper arrangement on the slider, the very same photolithographic process step is used to simultaneously define the opposing tips and the shadow mask (to be moved closely above the tips). This on-chip mask approach enables small gaps (800 nm) to be achieved between the shadow mask and the SWNT. Needle-like contacts are formed from metal deposited on the suspended nanotube using the nanotube itself as a template. The metal lead, with a width of less than 10 nm, is therefore efficiently self-aligned without the need for the exact location of the nanotube to be mapped, which would be necessary if electron-beam lithography were being used.

The gate coupling, represented by the 230 mV dec^{-1} subthreshold swing of D1, is remarkable because of the gap being large and the air in the gap being a weak dielectric. The good gate coupling can be attributed to the high electrical fields at the SWNT–metal junction due to the electrode geometry comprising nano-needles[13] on microtapered[23] poly-Si supports, minimizing screening of the gate. Simplified finite-element calculations indicate an enhancement by a factor of more than 60 of the electric field when compared to block-shaped supports (Supplementary Fig. S3).

The tiny hysteresis demonstrated here is a key advantage of the ultraclean suspended nanotubes being in contact only with the protruding metal leads and hence not disturbed by charge traps at the substrate and/or by polar molecules such as water[12]. The suspended, tapered contact geometry avoids the occurrence of hysteresis-inducing oxides[12, 15, 20] near the transistor channel. In particular for barrier-type transistors where the switching takes place at the contacts, we suggest that eliminating (or covering with metal) all non-conductive material close to the contacts is essential to omit hysteresis arising from charge injection[24]. We believe that in humid air the combination of low-defect SWNTs (Supplementary Figs S4,S5) and the omission of organic contamination[25] originating from resist-based lithography or from electron microscopy is crucial to avoid hysteresis. The observation of a minute level of hysteresis supports the results of density-functional calculations, which predict that the doping effect of H_2O from simple physisorption directly on clean SWNTs is negligible, so H_2O is assumed to be only indirectly[26], in the presence of oxides or other barriers, a source of hysteresis. With the availability of a suspended hysteresis-free system, experiments can be envisaged that address the issue of the origins of hysteresis by inducing defects, contamination or dielectrics.

The major concern regarding shadow masking at the nanoscale is blurring due to surface diffusion (Supplementary Fig. S6). However, favourable palladium clustering at the outermost SWNT–metal interface seems to occur, leading to a distinct onset of the electrodes (Fig. 4c). Future research could seek to reduce the area used (the area of the current design is 110 μm × 290 μm), as well as catalyst definition throughput and the yield of single-SWNT devices (see Supplementary Discussion for possible solutions).

Methods

MEMS chip with movable on-chip shadow mask

The sacrificial silicon oxide layers of the surface micromachined poly-Si MEMS (PolyMUMPs, MEMSCAP) were etched for 5 min in 40% HF. After release, the shadow mask slider became movable in-plane while being constricted in the vertical direction by a poly-Si layer. Dimple structures reduced the vertical play required for movability to a minimum.

Electron-beam lithography patterned catalyst and SWNT synthesis

To constrict nanotube growth to single spots on the poly-Si tips, catalyst islands were patterned by electron-beam lithography (Raith 150^{TWO}) using copolymer methylmethacrylate/methylacrylic acid. For catalyst formation, iron-loaded ferritin was adsorbed from aqueous solution[27], followed by resist lift-off. SWNT growth took place in a CH_4 + H_2 (155 mbar + 65 mbar) atmosphere for 15 min (PEO-603-PLC-300C, ATV Technologie). It is important to have the shadow-mask slider in its initially retracted position to prevent nanotubes from bridging to the shadow mask during growth.

Micromanipulation of guided shadow masks

The slider of the shadow mask was moved laterally by an atomic force microscopy (AFM) tip mounted on a probe stage equipped with piezo actuators. Poly-Si springs kept the shadow-mask slider in position during retraction of the AFM tip. While operating the light microscope in differential interference contrast mode, colour changes of the AFM cantilever helped to detect touchdown of the AFM tip on the sample surface. Because the shadow mask originates from the same

poly-Si layer as the tips used for SWNT integration, misalignment between the tips and the shadow mask at its initial position cannot occur. To allow the shadow mask to be placed close above the tips, it was formed on top of poly-Si spacer layers coated with a sacrificial layer. The tips were also at a lower elevation, realized by using thinned sacrificial SiO_2 layers. To ensure precise mechanical positioning of the shadow mask, cones and bumpers were formed simultaneously in the same photolithographic step.

Physical vapour deposition

Electron-beam evaporation (Univex 500, Leybold) of palladium was carried out at a base pressure of 9×10^{-8} mbar. The axis of sample rotation could be tilted with respect to the direction of material flux. The source to sample distance was 40 cm.

Instruments

SEM images were recorded using a Zeiss ULTRA 55 field-emission instrument. TEM imaging was performed with a FEI CM12 instrument with the acceleration voltage set to 100 kV. Electrical characterization was carried out using a computerized Keithley S4200SCS at a probe station.

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Contributions

M.M. devised the shadow mask concept and performed the experiments. L.D., T.H. and S.-W.L. contributed to catalyst preparation, electron-beam lithography and SWNT growth. C.R. contributed to discussions and simulations. C.H. initiated the research and contributed to discussions and conclusions. All authors discussed the results and commented on the manuscript.

Competing financial interests

The authors declare no competing financial interests.

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Supplementary information

PDF files

1. Supplementary information (3,034 KB)
   Supplementary information

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